INTERSIL

ICL8240, ICL8250, ICL8260 Programmable Timers/Counters

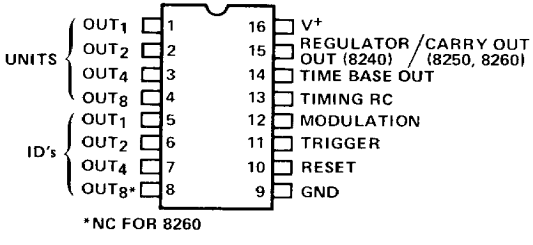
FEATURES

- Times from microseconds to minutes, hours, or days
- Time base set by simple R, C network or external clock
- Programmable with standard thumbwheel switches
- Select output count from
  - 1 RC to 255 RC (8240)
  - 1 RC to 99 RC (8250)
  - 1 RC to 59 RC (8260)
- Easily expanded to multiple decades (1 RC to 9,999 RC)
- Open collector outputs for flexibility
- High accuracy: ±0.5% typical
- Low drift: ±100ppm/°C typical
- Works over large supply range: 4V to 18V
- TTL compatible trigger and reset inputs

APPLICATIONS

- Programmable timing
  - Process timers
  - Appliance timers
  - Darkroom timers
- Programmable counter
  - Inventory/loading/filling
  - Counting/summing
- Frequency generation
  - Music synthesis
  - Harmonic synchronization
- Accurate, long-delay generator
- A/D conversion
- Digital Sample and Hold
- Pattern generation

PIN DIAGRAM



*NC FOR 8260

GENERAL DESCRIPTION

The 8240, 8250 and 8260 are a family of monolithic programmable timer circuits. They are intended to simplify the problem of selecting various time delays or frequency outputs available from a fixed oscillator circuit.

Each device consists of an accurate, low-drift oscillator a counter section of master-slave flip flops and appropriate logic and control circuitry all on one monolithic chip. The internal time base oscillator can be set with an external RC or can be disabled and the time base supplied from an external clock. The counter output taps are open collector transistors which can be programmed by a wire AND at external pins. Manual programming is easily accomplished by using standard thumbwheel switches. Additional logic circuitry will allow timing to be programmed by computer or microprocessor. These units are also very useful for generating ultra long delay times with relatively inexpensive RC components.

The 8260 is specifically designed to time accurate delays in seconds, minutes and hours. With its maximum count of 59 and carry out gate, a cascade of three 8260's will generate a one second clock from the 60 Hertz line, 60 seconds per minute and 60 minutes per hour programmable start to stop time. Thumbwheel switches with digits 0 to 5 and 0 to 9 are readily available to simplify the man-machine interface.

The 8250 is optimized for decimal counting and delays. It can be programmed by standard binary coded decimal (BCD) thumbwheel switches (0 to 9). Each unit gives 2 decades of counting allowing selection of time delays of from 1 RC to 99 RC. The carryout gate on the 8250 allows expansion to 9,999 or more.

The 8240 uses straight binary counting. With eight flip flops dividing down the base frequency, 8 suboctaves of the fundamental are available simultaneously in the astable mode. In the monostable mode the collectors can be wired AND to give any combination of pulse width of from 1 RC to 255 RC.

Applications for these versatile devices include appliance timers, darkroom timers and process timers. They can also be used as programmable counters. The internal clock can be disabled and the unit will count external pulses for programmable summing, loading or inventory applications. The internal clock can also be synchronized with the (m)th harmonic of an external sync and with the selectable counter, can provide a large number of non-harmonic frequencies from a single reference. Finally, they can be used as logic controlled switches in ramp type D-to-A and A-to-D converters.

ORDERING INFORMATION

TYPE	MAXIMUM COUNT	TEMPERATURE RANGE	16 PIN PACKAGE	ORDER PART NUMBER
8240C	255	0°C to +75°C	Plastic DIP	ICL 8240 C PE
8240M	255	-55°C to +125°C	Ceramic DIP	ICL 8240 M DE
8250C	99	0°C to +75°C	Plastic DIP	ICL 8250 C PE
8250M	99	-55°C to +125°C	Ceramic DIP	ICL 8250 M DE
8260C	59	0°C to +75°C	Plastic DIP	ICL 8260 C PE
8260M	59	-55°C to +125°C	Ceramic DIP	ICL 8260 M DE

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 18V
Power Dissipation
Ceramic Package 750mW
Derate above +25°C ..... 6mW/°C
Plastic Package 625mW
Derate above +25°C ..... 5.0mW/°C

Operating Temperature
8240M, 8250M, 8260M ..... −55°C to +125°C
8240C, 8250C, 8260C ..... 0°C to +75°C
Storage Temperature ..... −65°C to +150°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: See Figure 2, $V^+ = 5V$, $T_A = 25°C$, $R = 10k\Omega$, $C = 0.1\mu F$, unless otherwise noted.

PARAMETERS	8240M MIN.	8240M TYP.	8240M MAX.	8240C MIN.	8240C TYP.	8240C MAX.	UNITS	CONDITIONS
GENERAL CHARACTERISTICS								
Supply Voltage	4		18	4		18	V	For $V^+ < 4.5V$, Short Pin 15 to Pin 16
Supply Current								
Total Circuit (Reset)		3.5	6		4	7	mA	$V^+ = 5V$, $V_{TR} = 0$, $V_{RS} = 5V$
		12	16		13	18		$V^+ = 15V$, $V_{TR} = 0$, $V_{RS} = 5V$
Total Circuit (Trigger)		24			24			$V^+ = 15V$, $V_{TR} = 5V$, $V_{RS} = 0$ All outputs ON. (Worst Case)
Counter Only		1			1.5			See Figure 3, 8240 only
Regulator Output, V_R	4.1	4.4		3.9	4.4		V	Measured at Pin 15, $V^+ = 5V$
(8240 only)	6.0	6.3	6.6	5.8	6.3	6.8		$V^+ = 15V$, See Figure 4
TIME BASE SECTION								See Figure 2
Timing Accuracy		0.5	2.0		0.5	5	%	$V_{RS} = 0$, $V_{TR} = 5V$, Note 1.
Temperature Drift		150	300		200		ppm/°C	$V^+ = 5V$ Over Operating Temperature
		80			80			$V^+ = 15V$
Supply Drift		0.05	0.2		0.08	0.3	%/V	$V^+ \geq 8$ Volts, See Figure 11
Max. Frequency	100	130			130		kHz	$R = 1k\Omega$, $C = 0.007\mu F$
Time Base Output								Measured at Pin 14
V_{TB} High	2.4	2.8		2.4	2.8		V	$I_{Source} = 80\mu A$
V_{TB} LOW		0.2	0.4		0.2	0.4		$I_{Sink} = 3.2mA$
Modulation Voltage Level	3.00	3.50	4.0	2.80	3.50	4.20		Measured at Pin 12 $V^+ = 5V$
		10.5			10.5			$V^+ = 15V$
Recommended Range of Timing Components								See Figure 8
Timing Resistor, R	0.001		10	0.001		10	MΩ	
Timing Capacitor, C	0.007		1000	0.01		1000	μF	
TRIGGER/RESET CONTROLS								
Trigger								
Trigger Threshold		1.4	2.0		1.4	2.0	V	Measured at Pin 11
Trigger Current		8			10		μA	$V_{RS} = 0$, $V_{TR} = 2V$
Impedance		25			25		kΩ	
Response Time		1			1		μsec.	Note 2
Reset								
Reset Threshold		1.4	2.0		1.4	2.0	V	Measured at Pin 10
Reset Current		8			10		μA	$V_{TR} = 0$, $V_{RS} = 2V$
Impedance		25			25		kΩ	
Response Time		0.8			0.8		μsec.	Note 2
COUNTER SECTION								See Figue 4, $V^+ = 5V$
Max. Toggle Rate	0.8	1.5			1.5		MHz	$V_{RS} = 0$, $V_{TR} = 5V$ Max Input to Pin 14
Input:								
Impedance		15			15		kΩ	Measured at Pin 14
Threshold	1.0	1.4		1.0	1.4		V	
Output:								Measured at Pins 1 thru 8
Rise Time		180			180		nsec.	$R_L = 3k$, $C_L = 10pf$
Fall Time		180			180			
V_{OUT} Low		0.2	0.4		0.2	0.4	V	$I_{SINK} = 3.2mA$
Leakage Current		0.01	8		0.01	15	μA	$V_{OH} = 15V$

NOTE 1: Timing error solely introduced by 8240, measured as % of ideal time-base period of T = 1.00 RC.
NOTE 2: Propagation delay from application of trigger (or reset) input to corresponding state change in counter output at Pin 1.

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: See Figure 2, $V^+ = 5V$, $T_A = 25°C$, $R = 10k\Omega$, $C = 0.1\mu F$, unless otherwise noted.

PARAMETERS	8205M MIN.	8205M TYP.	8205M MAX.	8205C MIN.	8205C TYP.	8205C MAX.	UNITS	CONDITIONS
GENERAL CHARACTERISTICS								
Supply Voltage	4.5		18	4.5		18	V	
Supply Current								
Total Circuit (Reset)		3.5	6		4	7	mA	$V^+ = 5V$, $V_{TR} = 0$, $V_{RS} = 5V$
		12	16		13	18		$V^+ = 15V$, $V_{TR} = 0$, $V_{RS} = 5V$
Total Circuit (Trigger)		24			24			$V^+ = 15V$, $V_{TR} = 5V$, $V_{RS} = 0$ All outputs ON. (Worst Case)
TIME BASE SECTION								See Figure 2
Timing Accuracy		0.5	2.0		0.5	5	%	$V_{RS} = 0$, $V_{TR} = 5V$, Note 1
Temperature Drift		150	300		200		ppm/°C	$V^+ = 5V$ Over Operating Temp.
		80			80			$V^+ = 15V$
Supply Drift		0.05	0.2		0.08	0.3	%/V	$V^+ \geq 8$ Volts, See Figure 11
Max. Frequency	100	130			130		kHz	$R = 1k\Omega$, $C = 0.007\ \mu F$
Time Base Output								
V_{TB} HIGH	2.4	2.8		2.4	2.8		V	Measured at Pin 14 $I_{SOURCE} = 80\mu A$
V_{TB} LOW		0.2	0.4		0.2	0.4		$I_{SINK} = 3.2mA$
Modulation Voltage Level	3.00	3.50	4.0	2.80	3.50	4.20		Measured at Pin 12 $V^+ = 5V$
		10.5			10.5			$V^+ = 15V$
Recommended Range of Timing Components								
Timing Resistor, R	0.001		10	0.001		10	MΩ	See Figure 8
Timing Capacitor, C	0.007		1000	0.01		1000	μF	
TRIGGER/RESET CONTROLS								
Trigger								
Trigger Threshold		1.4	2.0		1.4	2.0	V	Measured at Pin 11
Trigger Current		8			10		μA	$V_{RS} = 0$, $V_{TR} = 2V$
Impedance		25			25		kΩ	
Response Time		1			1		μsec.	Note 2
Reset								
Reset Threshold		1.4	2.0		1.4	2.0	V	Measured at Pin 10
Reset Current		8			10		μA	$V_{TR} = 0$, $V_{RS} = 2V$
Impedance		25			25		kΩ	
Response Time		0.8			0.8		μsec.	Note 2
COUNTER SECTION								See Figure 4, $V^+ = 5V$
Max. Toggle Rate	0.8	1.5			1.5		MHz	$V_{RS} = 0$, $V_{TR} = 5V$ Max. Input Pin 14
Input:								
Impedance		15			15		kΩ	Measured at Pin 14
Threshold	1.0	1.4		1.0	1.4		V	
Output:								
Rise Time		180			180		nsec.	Measured at Pins 1 thru 8 $R_L = 3k$, $C_L = 10pF$
Fall Time		180			180			
V_{OUT} Low		0.2	0.4		0.2	0.4	V	$I_{SINK} = 3.2mA$
Leakage Current		0.01	8		0.01	15	μA	$V_{OH} = 15V$
CARRY OUT GATE								See Figure 4, $V^+ = 5V$
Vco Low		0.2	0.4		0.2	0.4	V	Measured on Pin 15 $I_{SINK} = 3.2mA$
Vco High	2.4	3.5		2.4	3.5			$I_{SOURCE} = 80\mu A$

NOTE 1: Timing error solely introduced by 8250, measured as % of ideal time-base period of T = 1.00 RC.
NOTE 2: Propagation delay from application of trigger (or reset) input to corresponding state change in counter output at Pin 1.

6

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: See Figure 2, $V^+ = 5V$, $T_A = 25°C$, $R = 10k\Omega$, $C = 0.1\mu F$, unless otherwise noted.

PARAMETERS	8260M MIN.	8260M TYP.	8260M MAX.	8260C MIN.	8260C TYP.	8260C MAX.	UNITS	CONDITIONS
GENERAL CHARACTERISTICS								
Supply Voltage	4.5		18	4.5		18	V	
Supply Current								
Total Circuit (Reset)		3.5	6		4	7		$V^+ = 5V$, $V_{TR} = 0$, $V_{RS} = 5V$
		12	16		13	18	mA	$V^+ = 15V$, $V_{q4TR} = 0$, $V_{RS} = 5V$
Total Circuit (Trigger)		24			24			$V^+ = 15V$, $V_{TR} = 5V$, $V_{RS} = 0$ All outputs ON. (Worst Case)
TIME BASE SECTION								See Figure 2
Timing Accuracy		0.5	2.0		0.5	5	%	$V_{RS} = 0$, $V_{TR} = 5V$, Note 1
Temperature Drift		150	300		200		ppm/°C	$V^+ = 5V$ Over Operating Temp.
		80			80			$V^+ = 15V$
Supply Drift		0.05	0.2		0.08	0.3	%/V	$V^+ \geq 8$ Volts, See Figure 11
Max. Frequency	100	130			130		kHz	$R = 1k\Omega$, $C = 0.007\mu F$
Time Base Output								Measured at Pin 14
V_{TB} HIGH	2.4	2.8		2.4	2.8			$I_{Source} = 80\mu A$
V_{TB} LOW		0.2	0.4		0.2	0.4	V	$I_{Sink} = 3.2mA$
Modulation Voltage								Measured at Pin 12
Level	3.00	3.50	4.0	2.80	3.50	4.20		$V^+ = 5V$
		10.5			10.5			$V^+ = 15V$
Recommended Range of Timing Components								See Figure 8
Timing Resistor, R	0.001		10	0.001		10	MΩ	
Timing Capacitor, C	0.007		1000	0.01		1000	μF	
TRIGGER/RESET CONTROLS								
Trigger								Measured at Pin 11
Trigger Threshold		1.4	2.0		1.4	2.0	V	
Trigger Current		8			10		μA	$V_{RS} = 0$, $V_{TR} = 2V$
Impedance		25			25		kΩ	
Response Time		1			1		μsec.	Note 2
Reset								
Reset Threshold		1.4	2.0		1.4	2.0	V	Measured at Pin 10
Reset Current		8			10		μA	$V_{TR} = 0$, $V_{RS} = 2V$
Impedance		25			25		kΩ	
Response Time		0.8			0.8		μsec.	Note 2
COUNTER SECTION								See Figure 4, $V^+ = 5V$
Max. Toggle Rate	0.8	1.5			1.5		MHz	$V_{RS} = 0$, $V_{TR} = 5V$ Max Input Pin 14
Input:								
Impedance		20			20		kΩ	Measured at Pin 14
Threshold	1.0	1.4		1.0	1.4		V	
Output:								Measured at Pins 1 thru 7
Rise Time		180			180		nsec.	$R_L = 3k$, $C_L = 10pF$
Fall Time		180			180			
V_{OUT} Low		0.2	0.4		0.2	0.4	V	$I_{SINK} = 3.2mA$
Leakage Current		0.01	8		0.01	15	μA	$V_{OH} = 15V$
CARRY OUT GATE								See Figure 4, $V^+ = 5V$
V_{CO} Low		0.2	0.4		0.2	0.4	V	Measured on Pin 15 $I_{SINK} = 3.2mA$
V_{HIGH}	2.4	3.5		2.4	3.5			$I_{SOURCE} = 80\mu A$

NOTE 1: Timing error solely introduced by 8260, measured as % of ideal time-base period of T = 1.00 RC.
NOTE 2: Propagation delay from application of trigger (or reset) input to corresponding state change in counter output at Pin 1.

BLOCK DIAGRAM

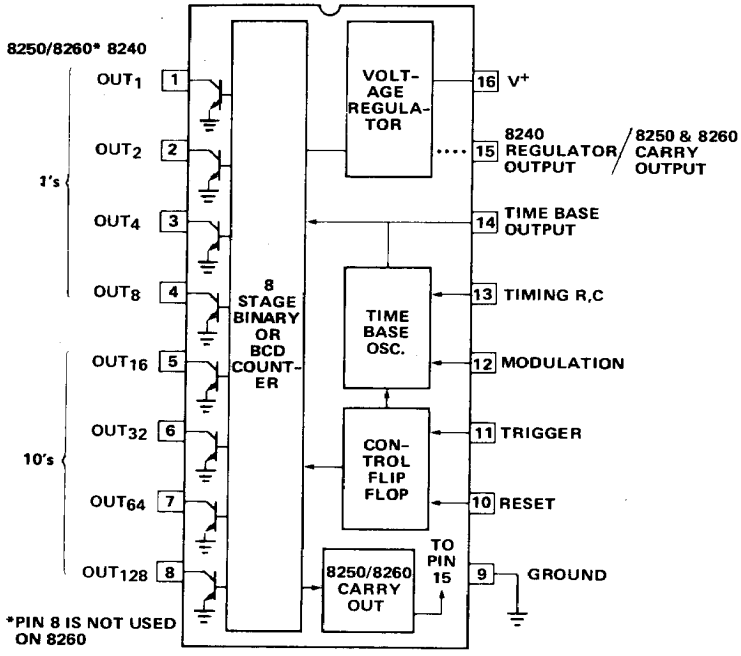


FIGURE 1.

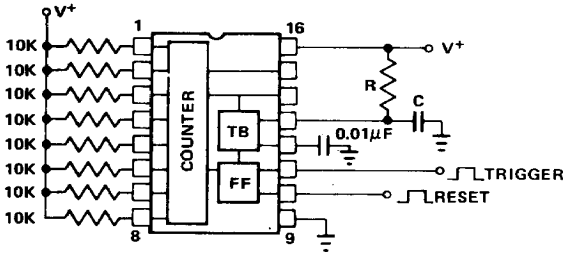


FIGURE 2: Generalized Test Circuit

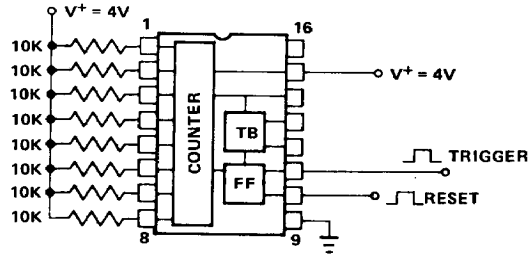


FIGURE 3: Test Circuit for Low-Power Operation (Time-Base Powered Down) 8240 Only

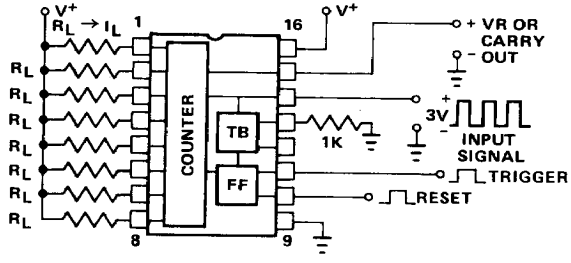


FIGURE 4: Test Circuit for Counter Section

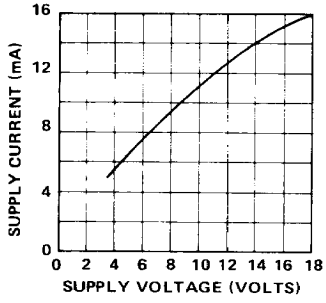


FIGURE 5: Supply Current vs. Supply Voltage in Reset Condition

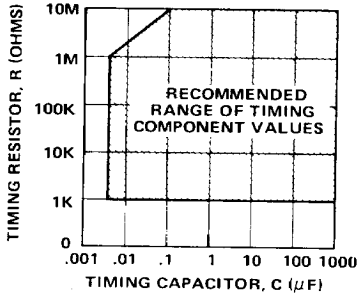


FIGURE 6: Recommended Range of Timing Component Values

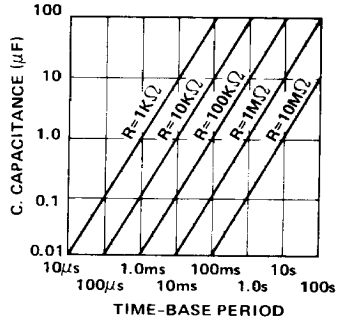


FIGURE 7: Time-Base Period, T, as a Function of External RC

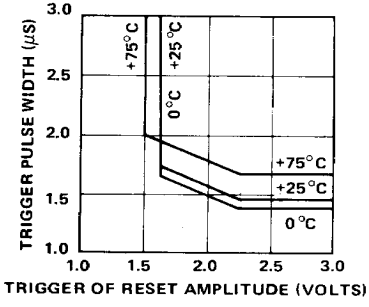


FIGURE 8: Minimum Trigger and Reset Pulse Widths at Pins 10 and 11

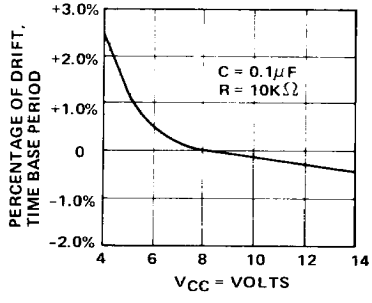


FIGURE 9: Power Supply Drift

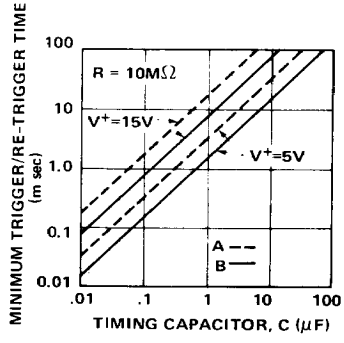


FIGURE 10:
A) Minimum Trigger Delay Time Subsequent to Application of Power
B) Minimum Re-trigger Time, Subsequent to a Reset Input

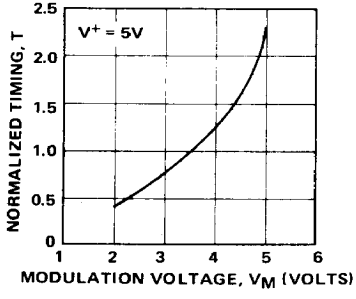


FIGURE 11: Normalized Change in Time-Base Period As a Function of Modulation Voltage at Pin 12

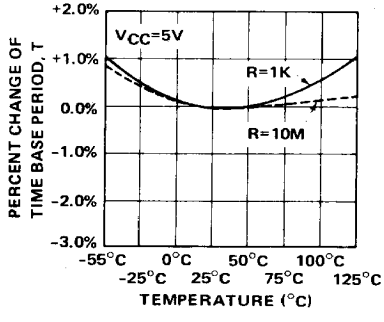


FIGURE 12: Temperature Stability at V_{CC} = 5V

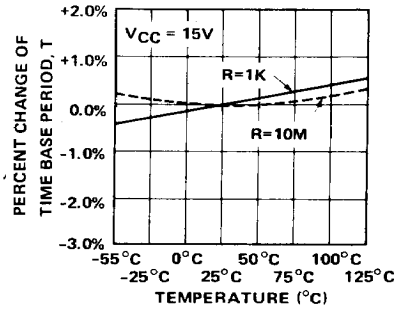


FIGURE 13: Temperature Stability at V_{CC} = 15V

6

INTRODUCTION TO PROGRAMMABLE TIMING

A timing diagram of waveforms and circuit states is shown in Figure 14. A generalized circuit connection for the 8240/50/60 is shown in Figure 15.

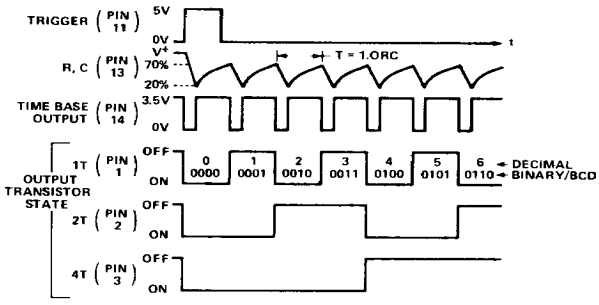


FIGURE 14: Timing Diagram of Output Waveforms (8240)
(**NOTE:** BCD States are not all symmetrical)

The timing cycle is initiated by applying a positive-going trigger pulse to pin 11. This trigger pulse enables the counter section, sets all counter outputs to the "low" or "on" state, and starts the time base oscillator. Then external C is charged through external R from 20% to 70% of V^+, generating a timing waveform with period, T, equal to 1 RC. A short negative clock or time base pulse occurs during the capacitor discharge portion of the waveform. (Normally this time is small compared with the period T but has been enlarged for Figure 14.) These clock pulses are counted by the binary counter of the 8240 or by a Binary Coded Decimal (BCD) Counter in the 8250/60. The timing cycle terminates when a positive-going reset pulse is applied to pin 10. When the circuit is at reset state, both the time base and the counter sections are disabled and all the counter outputs are at a "high" or "off" state. The carry-out is also high.

In most timing applications, one or more of the counter outputs are connected back to the reset terminal, as shown in Figure 15, with S_1 closed. In this manner, the circuit will start timing when a trigger is applied and will automatically reset itself to complete the timing cycle when a programmed count is completed. If none of the counter outputs are connected back to the reset terminal (switch S_1 open), the circuit would operate in its astable or free-running mode, subsequent to a trigger input.

PROGRAMMING CAPABILITY

The counter outputs (pins 1 through 8) are open-collector type stages and can be shorted together to a common pull-up resistor to form a "wired-and" connection. The combined output will be "low" as long as any one of the outputs is low. In this manner, the time delays associated with each counter output can be *summed* by simply shorting them together to a common output bus as shown in Figure 15. For example, if only pin 6 is connected to the output and the rest left open, the total duration of the timing cycle. T_O, would be 32T for an 8240, and 20T for an 8250. Similarly, if pins 1, 5, and 6 were shorted to the output bus, the total time delay would be $T_O = (1 + 16 + 32)\ T = 49T$ (8240) or $(1 + 10 + 20)\ T \pm 31T$ (8250). In this manner, by proper choice of counter terminals connected to the output bus, one can program the timing cycle to be:

$1T \leq T_O \leq 255T$ (8240)
$1T \leq T_O \leq 99T$ (8250)
$1T \leq T_O \leq 59T$ (8260)

Note that for the 8250 and 8260 invalid count states (BCD values ≥ 10) will not be recognized, and the counter will not stop.

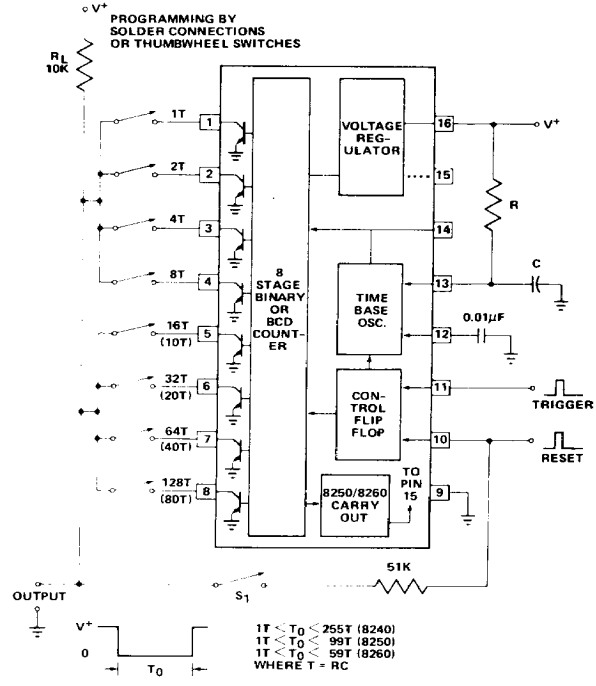


FIGURE 15: Generalized Circuit Connection for Timing Applications (Switch S_1 Open for Astable Operations, Closed for Monostable Operations)

THUMBWHEEL SWITCHES

While the 8240 is frequently hard wired for a particular function, the 8250 and 8260 can easily be programmed by using Thumbwheel switches. Standard BCD thumbwheel switches have four inputs (2^0, 2^1, 2^2, 2^3 or 1, 2, 4 and 8) and one "common", which are connected according to the binary equivalent of the digits 0 through 9.

For a single 8250 two such switches would select a time of from 01 RC to 99 RC. A cascade of two 8250's (using the carry out gate) would expand selection to 9999 RC. For an 8260 there are standard BCD Thumbwheel switches for the 0 through 5 digit (Twelve position, 0 to 5 repeated).

DESCRIPTION OF CIRCUIT CONTROLS

COUNTER OUTPUTS (PINS 1 THROUGH 8)

The binary counter outputs are buffered "open-collector" type stages, as shown in Figure 15. Each output is capable of sinking ≈ 5mA of load current. At reset condition, all the counter outputs are at high or non-conducting state. Subsequent to a trigger input, the outputs change state in accordance with the timing diagram of Figure 14.

The counter outputs can be used individually, or can be connected together in a wired-and configuration, as described in the Programming section.

GROUND (PIN 9)

This is the return or most negative supply for the device. It should have a very low impedance since capacitor discharge and other switched currents could create transients.

RESET AND TRIGGER INPUTS (PINS 10 AND 11)

The circuit is reset or triggered with positive-going control pulses applied to pins 10 and 11. The threshold level for these controls is approximately two diode drops (≈1.4V) above ground, and is therefore TTL/DTL compatible.

When power is applied to the 8240/50/60 with no trigger or reset inputs, the circuit reverts to "reset" state. Once triggered, the circuit is immune to additional trigger inputs, until the timing cycle is completed or a reset input is applied. If both the reset and the trigger controls are activated simultaneously, trigger overrides reset. Minimum pulse widths for reset and trigger inputs are shown in Figure 8.

MODULATION AND SYNC INPUT (PIN 12)

The period T of the time-base oscillator can be modulated by applying a dc voltage to this terminal (see Figure 11). The time-base oscillator can be synchronized to an external clock by applying a sync pulse to pin 12, as shown in Figure 26. Recommended sync pulse widths and amplitudes are also given in the figure.

TIMING TERMINAL (PIN 13)

The time-base period T is determined by the external RC network connected to this pin. When the time-base is triggered, the waveform at pin 13 is an exponential ramp with a period T = 1.0 RC. Figures 5 and 6 show RC values.

TIME-BASE OUTPUT (PIN 14)

Time-Base output is an open-collector type stage. An internal 10kΩ pull-up resistor is provided to ensure correct operation. At reset state, the time-base output is at "high" state. Subsequent to triggering, it produces a negative-going pulse train with a period T = RC, as shown in the diagram of Figure 14.

Time-base output is internally connected to the binary counter section and also serves as the input for the external clock signal when the circuit is operated with an external time-base.

The counter input triggers on the negative-going edge of the timing or clock pulses applied to pin 14. The trigger threshold for the counter section is ≈ +1.4 volts. The counter section can be disabled by clamping the voltage level at pin 14 to ground.

Under certain operating conditions such as high supply voltages (V+ > 7V) and small values of timing capacitor (C < 0.1μF) the pulse-width of the time-base output at pin 14 may be too narrow to trigger the counter section. This can be corrected by connecting a 300pF capacitor from pin 14 to ground.

CARRY OUTPUT (PIN 15, 8250 AND 8260 ONLY)

This pin will go HI for the last 10 counts of a 59 or 99 count, and can be used to drive another 8250 or 8260 counter stage, while still using all the counter outputs of the first. Thus, by cascading several 8250's a large BCD countdown can be achieved. The carry-out can also be used to drive TTL logic, etc.

REGULATOR OUTPUT (PIN 15, 8240 ONLY)

This terminal can serve as a V+ supply to additional 8240 circuits when several timer circuits are cascaded (see Figure 19), to minimize power dissipation. For circuit operation with external clock, pin 15 can be used as the V+ terminal to power-down the internal time-base and reduce power dissipation.

When the internal time-base is used with V+ ≤ 4.5V, pin 15 should be shorted to pin 16.

V+ (PIN 16)

This is the most positive supply voltage. (4.5V to 18V) A low supply impedance or 0.1μF to ground will help suppress voltage transients.

APPLICATIONS INFORMATION

PRECISION TIMING (Monostable Operation)

In precision timing applications, the 8240/50 is used in its monostable or "self-resetting" mode. The generalized circuit connection for this application is shown in Figure 16.

The output is normally "high" and goes to "low" subsequent to a trigger input. It stays low for the time duration T_O and then returns to the high state. The duration of the timing cycle T_O is given as:

$$T_O = NT = NRC$$

where T = RC is the time-base period as set by the choice of timing components at pin 13 (see Figure 7). N is an integer in the range of:

$$1 \leq N \leq 255\ (8240) \leq 99\ (8250) \leq 59\ (8260)$$

as determined by the combination of counter outputs (pins 1 through 8) connected to the output bus, as described before. (see page 7)

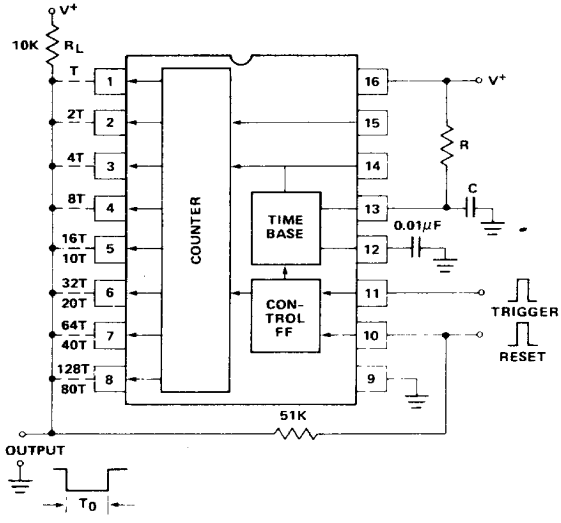


FIGURE 16: Circuit for Monostable Operation

6

ULTRA-LONG DELAY GENERATION

Two 8240/50/60 units can be cascaded as shown in Figure 17 to generate extremely long time delays. In this application, the reset and the trigger terminals of both units are tied together and the time base of Unit 2 disabled. In this manner, the output would normally be high when the system is at reset. Upon application of a trigger input, the output goes low for a total of $(256)^2$ or 65,536 cycles of the time-base oscillator (8240) or $(100)^2$ or 10,000 cycles (8250). The 8250/60 can also be connected as shown in Figure 18, allowing finer resolution in timing interval. The same applies to the 8260. PROGRAMMING: Total timing cycle of two cascaded 8240's can be programmed from T_O = 256RD to T_O = 65,536RC in 256 discrete steps by selectively shorting any one or the combination of the counter outputs from Unit 2 to the output bus. Two cascaded 8250's can be programmed from T_O = 1RC to T_O = 9999RC in 10,000 discrete steps by selectively shorting any combination of the counter outputs from both units to the output bus.

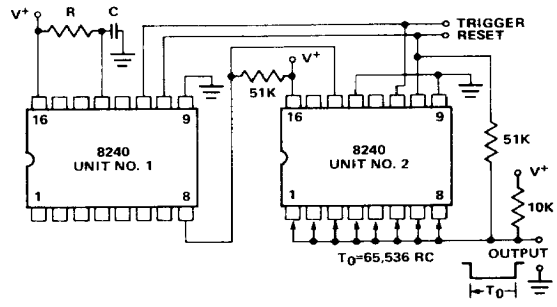


FIGURE 17: Cascaded Operation for Long Delay Generation (8240)

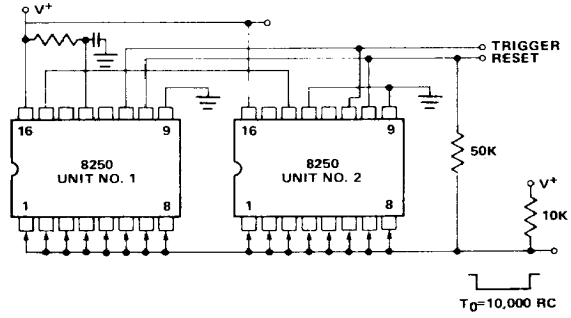


FIGURE 18: Cascaded Operation (8250 or 8260)

LOW-POWER OPERATION (8240 ONLY)

In cascaded operation, the time-base section of Unit 2 can be powered down to reduce power consumption, by using the circuit connection of Figure 19. In this case, the V+ terminal (pin 16) of Unit 2 is left open circuited, and the second unit is powered from the regulator output of Unit 1, by connecting pin 15 of both units. The V+ terminal of an 8250 can be connected to pin 15 of an 8240, but the power drain is not greatly reduced by this connection.

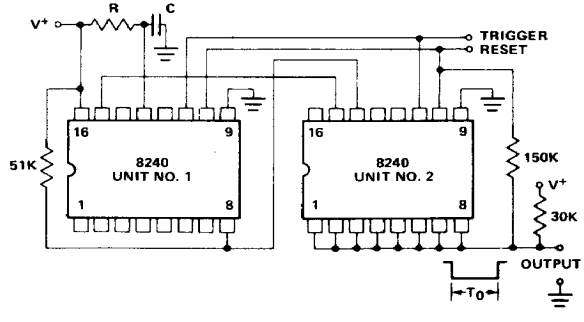


FIGURE 19: Low-Power Operation of Cascaded Timers (8240 only)

ELECTRONICALLY PROGRAMMED TIMER/COUNTER

The current interest in microprocessors, ROM's, PROM's, etc., requires timers which can be programmed electronically. Figures 20A and B show two ways of using readily available TTL/MSI logic to accomplish this. Although one is shown as a timer and the other as a counter, the choice of an external or internal clock would allow either circuit to perform either function.

The circuit of Figure 20A uses a standard 54/74 series TTL four bit magnitude comparator to compare the digitally programmed input with the 8240/50/60 counter outputs. The Greater, Less Than and Equal waveforms provide several outputs to choose from. An external start pulse triggers the timer and the A < B output is used as a reset.

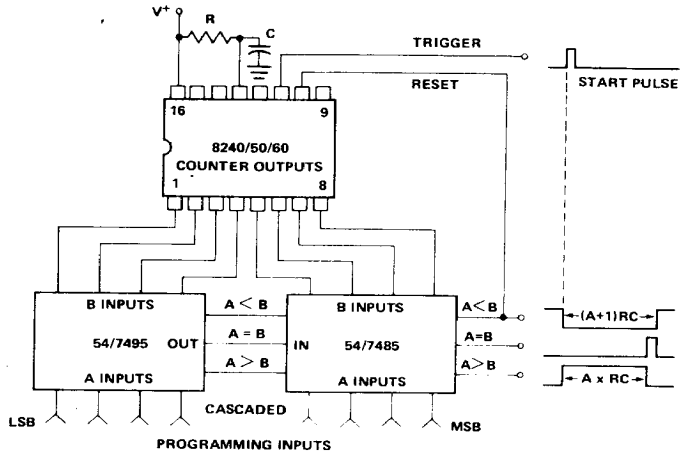


FIGURE 20A: Electronically Programmed Timer

In Figure 20B two Quad Nor circuits with open collector outputs are wired together to form an inexpensive digital comparator. A start pulse triggers the 8240/50/60 counter and sets the output flip flop high. The digital comparator output goes high momentarily when A = B. This resets the flip flop which in turn resets the counter. For extended temperature range or higher speed operation, individual pull-up resistors may be needed on the counter outputs of both circuits 20A and 20B.

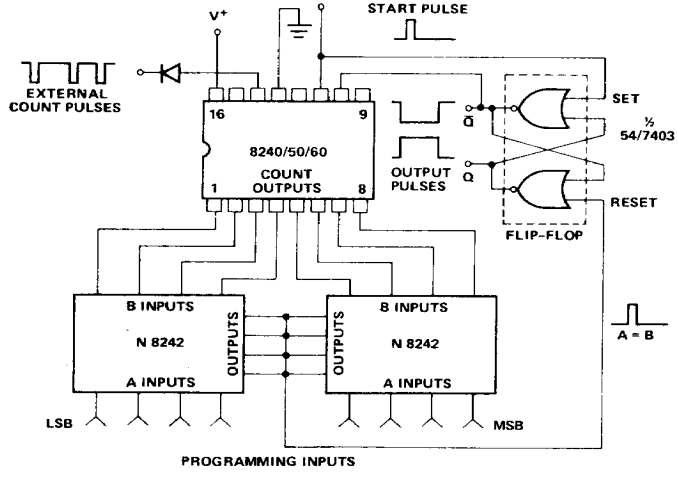


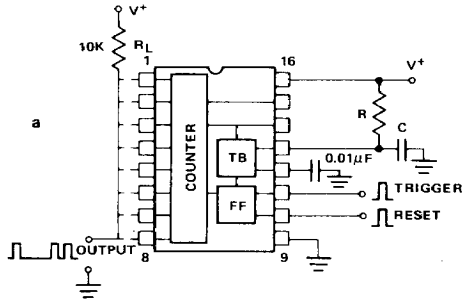
FIGURE 20B: Electronically Programmed Counter

ASTABLE OPERATION

The 8240/50 can be operated in its astable or free-running mode by disconnecting the reset terminal (pin 10) from the counter outputs. Two typical circuit connections for this mode of operation are shown in Figure 21. In the circuit connection of Figure 21(a), the circuit operates in its free-running mode, with external trigger and reset signals. It will start counting and timing subsequent to a trigger input until an external reset pulse is applied. Upon application of a positive-going reset signal to pin 10, the circuit reverts back to its rest state. The circuit of Figure 21(a) is essentially the same as that of Figure 15, with the feedback switch S_1 open.

The circuit of Figure 21(b) is designed for continuous operation. The circuit self-triggers automatically when the power supply is turned on, and continues to operate in its free-running mode indefinitely.

In astable or free-running operation, each of the counter outputs can be used individually as synchronized oscillators; or they can be interconnected or generate complex pulse patterns.



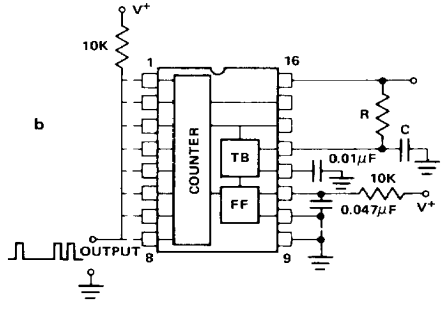


FIGURE 21: Circuit Connections for Astable Operation
(a) Operation with External Trigger and Reset Controls
(b) Free-running or Continuous Operation

BINARY OR DECIMAL PATTERN GENERATION

In astable operation, as shown in Figure 21, the output of the 8240/50 appears as a complex pulse pattern. The waveform of the output pulse train can be determined directly from the timing diagram of Figure 14 which shows the phase relations between the counter outputs. Figure 22 shows some of these complex pulse patterns. The pulse pattern repeats itself at a rate equal to the period of the *highest* counter bit connected to the common output bus. The minimum pulse width contained in the pulse train is determined by the *lowest* counter bit connected to,the output.

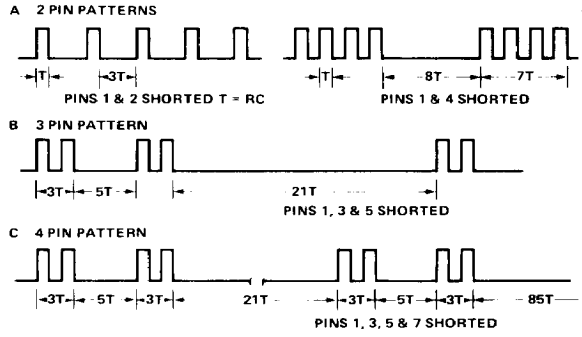


FIGURE 22: Pulse Patterns Obtained by Shorting Various Counter Outputs (Shown for the 8240)

OPERATION WITH EXTERNAL CLOCK

The 8240/50 can be operated with an external clock or time-base, by disabling the internal time-base oscillator and applying the external clock input to pin 14. The recommended circuit connection for this application is shown in Figure 23. The internal time-base can be de-activated by connecting pin 13 to ground. The counters are triggered on the negative-going edges of the external clock pulse. For proper operation, a minimum clock pulse amplitude of 3 volts is required. Minimum external clock pulse width is 1μs.

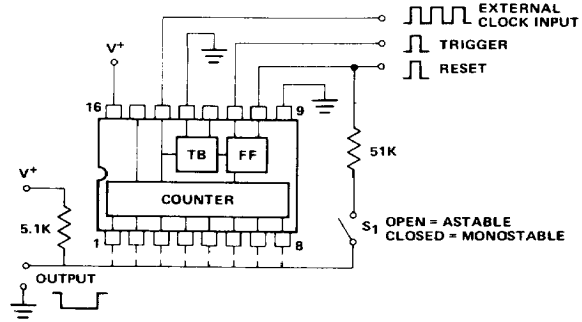


FIGURE 23: Operation with External Clock

FREQUENCY SYNTHESIZER

The programmable counter section of 8240/50 can be used to generate many discrete frequencies from a given time base setting using the circuit connection of Figure 24. The output of the circuit is a positive pulse train with a pulse width equal to T, and a period equal to (N + 1) where N is the programmed count in the counter.

The modulus N is the *total count* corresponding to the counter outputs connected to the output bus. Thus, for example, if pins 1, 3 and 6 are connected together to the output bus, the total count is: N = 1 + 4 + 32 = 37 and the period of the output waveform is equal to (N + 1) T or 38T (25T for 8250). In this manner, many different frequencies can be synthesized from a given time-base setting.

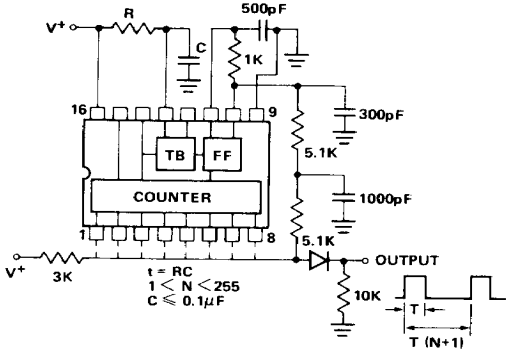


FIGURE 24: Frequency Synthesis from Internal Time-Base

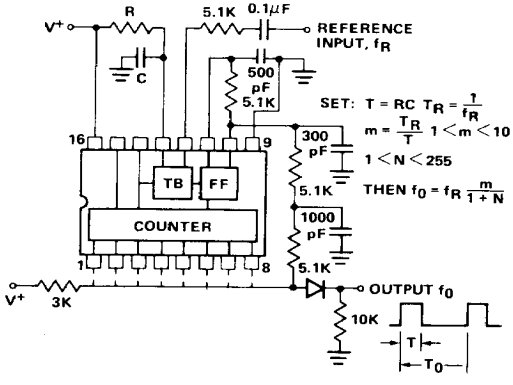


FIGURE 25: Frequency Synthesis by Harmonic Locking to an External Reference

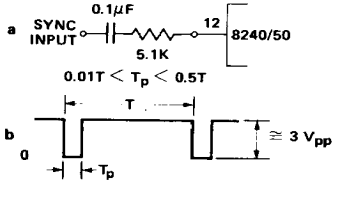


FIGURE 26: Operation with External Sync Signal.
(a) Circuit for Sync Input
(b) Recommended Sync Waveform

HARMONIC SYNCHRONIZATION

The time-base can be synchronized with *integer multiples or harmonics* of an input sync frequency, by setting the time-base period, T, to be an integer multiple of the sync pulse period, T_S. This can be done by choosing the timing components R and C at pin 13 such that:

$T = RC = (T_S/m)$ where
m is an integer, $1 \leq m \leq 10$.

Figure 27 gives the typical pull-in range for harmonic synchronization, for various values of harmonic modulus, m. For $m < 10$, typical pull-in range is greater than ±4% of time-base frequency. For $m > 10$, the circuit is too sensitive for reliable synchronization.

SYNTHESIS WITH HARMONIC LOCKING: The harmonic synchronization property of the 8240/50 time-base can be used to generate a wide number of discrete frequencies from a given input reference frequency. The circuit connection for this application is shown in Figure 25. (See Figures 26 and 27 for external sync waveform and harmonic capture range.) If the time base is synchronized to (m)th harmonic of input frequency where $1 \leq m \leq 10$, as described in the section on "Harmonic Synchronization", the frequency of f_o of the output waveform in Figure 25 is related to the input reference frequency f_R as:

$$f_o = f_R \frac{m}{(N + 1)}$$

where m is the harmonic number, and N is the programmed counter modulus. For a range of $1 \leq N \leq 255$, the circuit of Figure 19 can produce 2550 different frequencies from a single fixed reference.

One particular application of the circuit of Figure 25 is generating frequencies which are not harmonically related to a reference input. For example, by choosing the external RC to set m = 10 and setting N = 5, one can obtain a 100Hz output frequency synchronized to 60Hz power line frequency. See Figure 29.

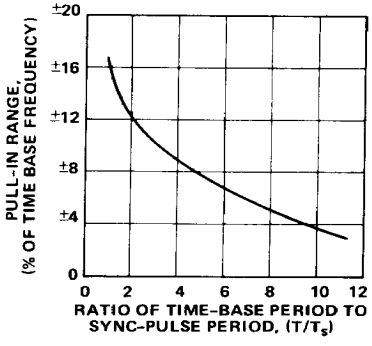


FIGURE 27: Typical Pull-In Range for Harmonic Synchronization

8260 APPLICATIONS

The 8260 provides a convenient method of generating accurate long delays where the inputs are programmed in terms of seconds, minutes and hours. An example of this is the 100 hour timer shown in Fig. 28. The 8260 on the right uses the carryout gate to generate a one second clock from a 60 hertz line source. The diodes on the time base input rectify the input signal and alternately clamp and release the internal pull up resistor at pin 14. The input network depends on the amplitude of 60 Hertz signal available. The internal oscillators are disabled with a 1K resistor to ground at pin 13.

The second and third 8260's are programmable with thumbwheel switches up to 59 seconds and 59 minutes. The carryout of each divider drives the next counter. An 8250 was chosen as the final stage to give a maximum count of 99 hours. All Reset pins are tied together and back to the 10K output pull up at the thumbwheel switches. The timing cycle begins by closing the push button to pulse the trigger inputs which are also tied together. The output is a normally high voltage which goes low when triggered. The output will stay low until the counters reach the time programmed at the thumbwheel switches. At that time the output returns to the high state and resets all the counters.

Some applications require monitoring of the continuing count. The Intersil ICM7045 (or 7208) provides a counter chip plus direct drive to seven segment LED displays. The counter can be reset from the 8260 (or 8250) timer after the programmed count is reached.

The timing resolution can be increased to hundredths of a second by substituting 8250's for the initial stages and using the 60 Hertz line to generate a 100 Hertz clock. This was shown in Figure 25 under synthesis with harmonic locking. See Figure 29.

For applications with no 60 Hertz signal available the Intersil ICM7049 is recommended. This part works with a 4Mhz quartz crystal to generate a very stable one pulse per second clock frequency. See Figure 30.

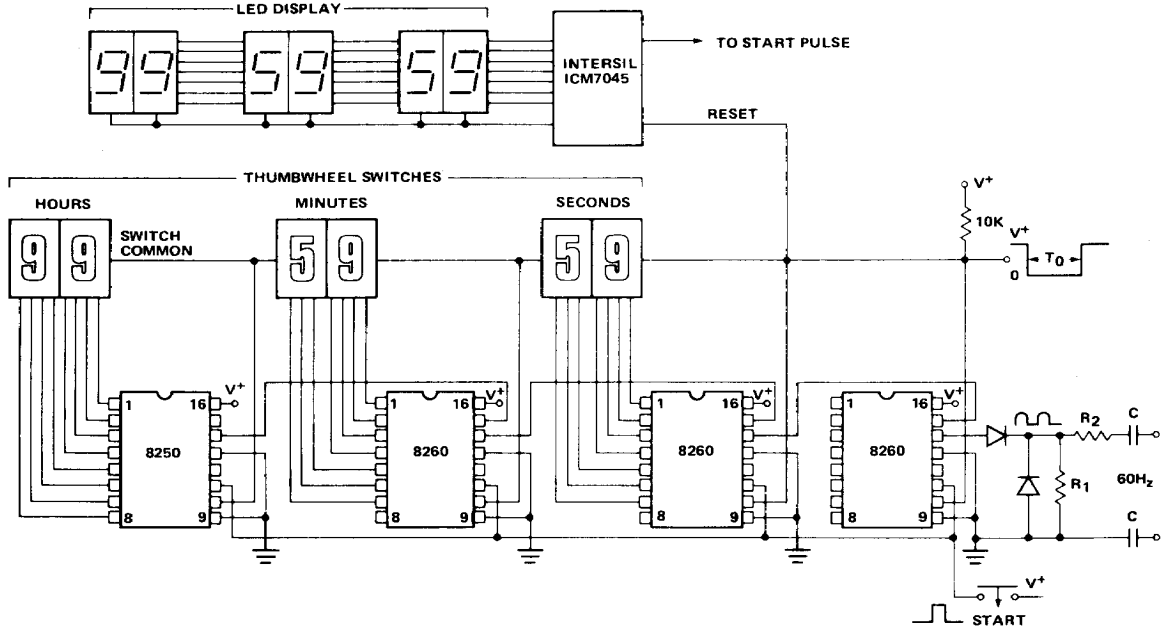


FIGURE 28: Programmable 100 Hour Timer with Display

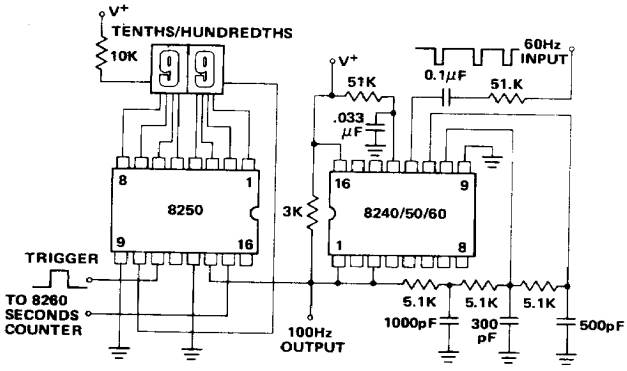


FIGURE 29: Front End for High Resolution Timer

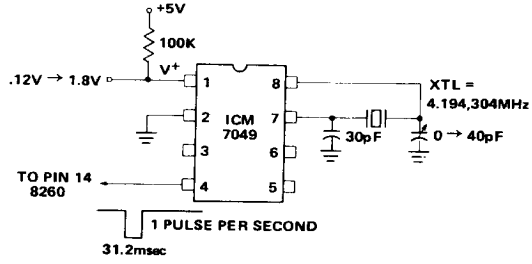


FIGURE 30: Intersil 7049 CMOS 1 Second Reference Oscillator

STAIRCASE GENERATOR

The open collector outputs of the 8240/50/60 counter stages are useful in several applications where digitally sequenced switches are needed. One example is the staircase generator of Figure 31. In this circuit an array of resistors is switched to ground to generate binary (or BCD) weighted currents. The op amp converts these currents to an output voltage. Under reset condition the switches are off and the output is at ground. When a trigger is applied the output goes to V_{REF} and generates a negative going staircase of 256 (or 100) levels. The time duration of each stop is equal to the time base period (T = RC). The amplitude of the staircase can be varied by changing the input reference voltage. The staircase can be stopped at any desired level by applying a "disable" signal to pin 14 as shown.

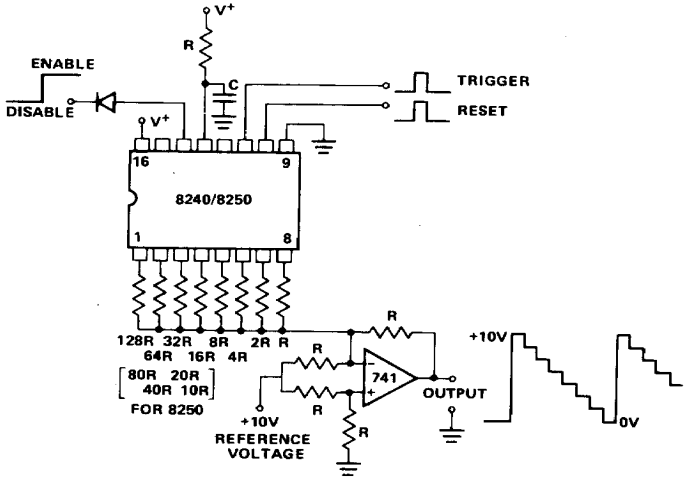


FIGURE 31: Staircase Generator

DIGITAL SAMPLE AND HOLD

By adding a comparator and RS flip flop to the staircase circuit we obtain the digital sample and hold shown in Figure 32. When a "strobe" input is applied, the 8240/8250 is first reset and then triggered through the small RC at pin 11 which delays the strobe signal. The strobe also sets the flip flop which in turn enables the counter via pin 14. The op amp goes to the high state and begins to count down at a rate set by the counter time base. When the op amp output reaches the analog input to be sampled; the comparator switches, resetting the flip flop and stops the count. The op amp output will accurately hold the sampled value until the next strobe pulse is applied. If the 8240/50 time base is set as shown, the maximum acquisition time would be 256 (or 100) times .01 msec, or approximately 2.6 msec.

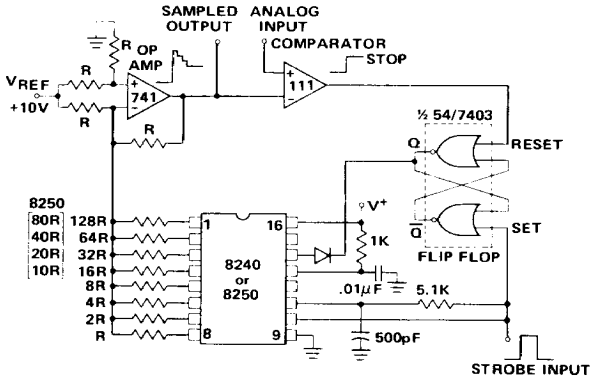


FIGURE 32: Digital Sample and Hold

ANALOG TO DIGITAL CONVERTER

Figure 33 shows an 8 bit binary (8240) or 2 digit BCD (8250) A/D converter using the staircase scheme of Figure 31. The operation is similar to the digital sample and hold of Figure 32 except digital outputs are taken off the counter output taps. In this circuit an input strobe pulse first resets then triggers the 8240/50 and sets the flip flop which enables the counter. The staircase from the op amp counts down until it reaches the analog input, at which time the comparator resets the flip flop and stops the count. The digital word at the 8 outputs is the complementary binary (or BCD) equivalent of the analog input. The maximum conversion time is again approximately 2.6 msec. The $\overline{Q}$ flip flop output is convenient to use as a data ready flag since its output goes high when the conversion is complete.

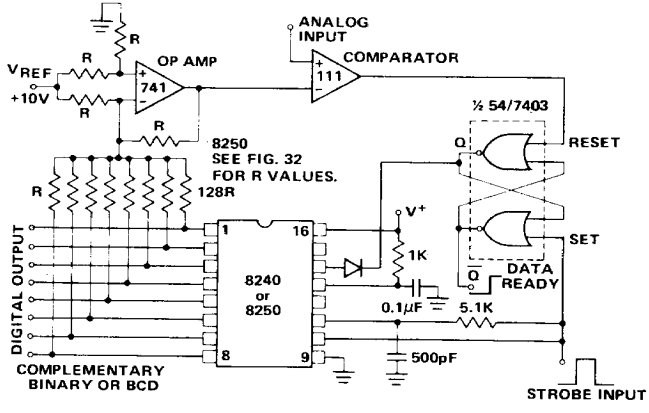
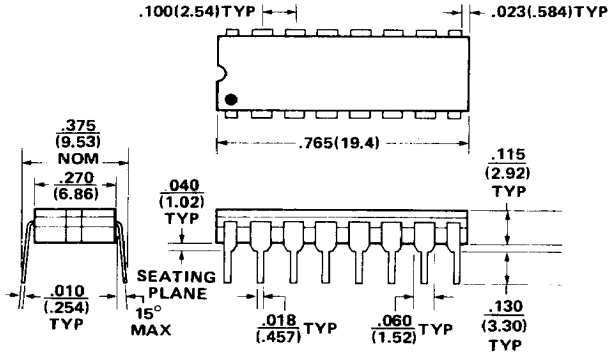


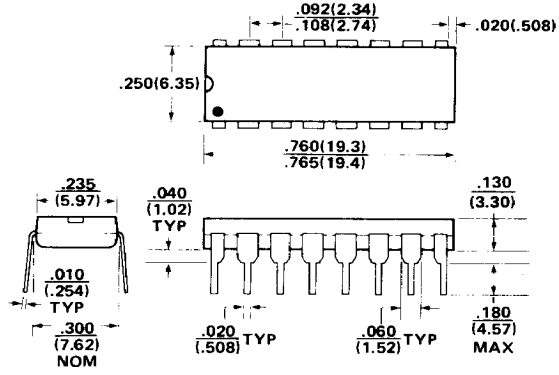
FIGURE 33: Analog-To-Digital Converter

PACKAGE DIMENSIONS

16 PIN CERAMIC DIP (DE)



16 PIN PLASTIC DIP (PE)



6