



# Lithium-Ion Battery Pack Protector

MAX1665S/V/X

## General Description

The MAX1665 provides protection against overvoltage, undervoltage, overcharge current, and overdischarge current for 2-cell to 4-cell lithium-ion (Li+) battery packs. Very low operating current ensures that cells are not overdischarged during long storage periods.

The MAX1665 controls two external N-channel MOSFETs to limit the charge and discharge voltages. Charging is allowed when the per-cell voltage is below +4.3V. When the voltage on any cell rises above +4.3V (overvoltage limit), the MAX1665 turns off the charge MOSFET. This safety feature prevents overcharge of any cell within the battery pack.

Discharge is allowed when the per-cell voltage is above +2.5V (undervoltage limit). If the voltage across any cell falls below +2.5V, the MAX1665 turns off the discharge MOSFET. This safety feature prevents overdischarge of any cell within the battery pack.

Charging and discharging are allowed if the voltage between PKN and BN is less than 250mV. This safety feature prevents excessive pack current.

## Applications

Lithium-Ion Battery Packs

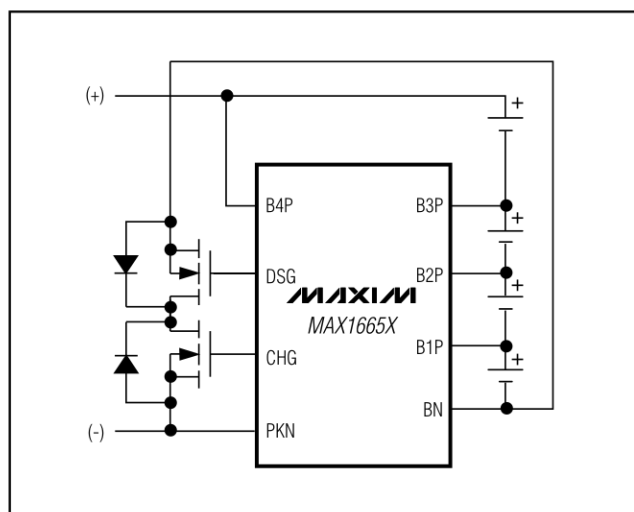
## Features

- ◆ Complete Protection Against:
  - Cell Overvoltage
  - Cell Undervoltage
- ◆ Pack Protection for Excessive Charge and Discharge
- ◆ Very Low Supply Current: 16 $\mu$ A typ
- ◆ Low Standby Current: 1 $\mu$ A max
- ◆ Matched Cell Input Bias Current (<500pA)  
Preserves Cell Balance

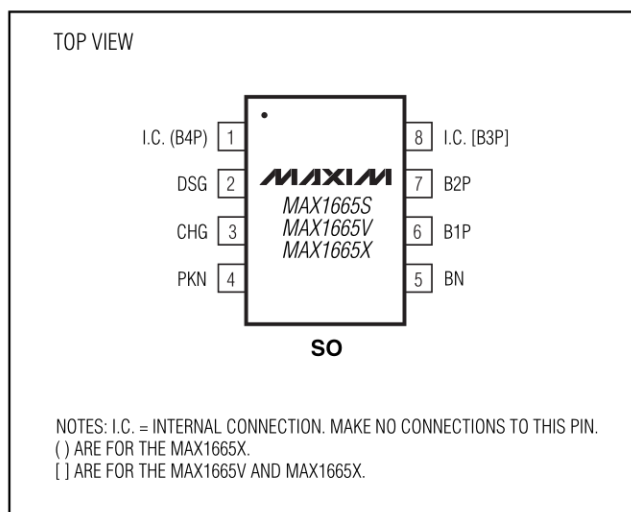
## Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	CELL COUNT
MAX1665SESA	-40°C to +85°C	8 SO	2
MAX1665VESA	-40°C to +85°C	8 SO	3
MAX1665XESA	-40°C to +85°C	8 SO	4

## Typical Operating Circuit



## Pin Configuration



# Lithium-Ion Battery Pack Protector

## ABSOLUTE MAXIMUM RATINGS

B4P to PKN (MAX1665X).....-0.3V to +24V  
 B3P to PKN (MAX1665V).....-0.3V to +18V  
 B2P to PKN (MAX1665S).....-0.3V to +12V  
 B1P to PKN, B2P to B1P, B3P to B2P, B4P to B3P...-0.3V to +6V  
 CHG to PKN, DSG to BN  
     MAX1665S.....-0.3V to ( $V_{B2P} + 0.3V$ )  
     MAX1665V.....-0.3V to ( $V_{B3P} + 0.3V$ )  
     MAX1665X.....-0.3V to ( $V_{B4P} + 0.3V$ )  
 B2P to BN (MAX1665S).....-0.3V to +12V

B3P to BN (MAX1665V).....-0.3V to +18V  
 B4P to BN (MAX1665X).....-0.3V to +24V  
 Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )  
     8-Pin SO (derate 5.88mW/ $^\circ\text{C}$  above  $+70^\circ\text{C}$ ).....471mW  
 Operating Temperature Range .....-40 $^\circ\text{C}$  to +85 $^\circ\text{C}$   
 Junction Temperature.....+150 $^\circ\text{C}$   
 Temperature Range.....-65 $^\circ\text{C}$  to +150 $^\circ\text{C}$   
 Lead Temperature (soldering, 10s).....+300 $^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

( $V_{B2P} = 8V$  (MAX1665S),  $V_{B3P} = 12V$  (MAX1665V),  $V_{B4P} = 16V$  (MAX1665X),  $T_A = 0^\circ\text{C}$  to +85 $^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ\text{C}$ .)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
B2P Voltage Range	$V_{B2P}$	MAX1665S		4		10	V
B3P Voltage Range	$V_{B3P}$	MAX1665V		4		15	V
B4P Voltage Range	$V_{B4P}$	MAX1665X		4		20	V
Overvoltage Threshold	$V_{OV}$	Cell voltage rising		4.26	4.3	4.34	V
Overvoltage Hysteresis	$V_{CE}$				0.10		V
Undervoltage Threshold	$V_{UV}$			2.4	2.5	2.6	V
Undervoltage RESET	$V_{RE}$	$V_{BN} - V_{PKN}$		0	18	30	mV
Overcurrent Sense Threshold	$V_{CH}$			$\pm 200$	$\pm 250$	$\pm 300$	mV
Overcurrent Hysteresis	$V_{CH2}$				5		mV
Overvoltage/Undervoltage Delay	$t_{UV}$	(Note 1)			200		ms
Overcurrent Detection Delay	$t_{IO}$				10		ms
CHG, DSG Output Voltage High		$I_{OUT} = 100\mu\text{A}$	MAX1665S	$V_{B2P} - 1.8$	$V_{B2P} - 0.54$		V
			MAX1665V	$V_{B3P} - 1.8$	$V_{B3P} - 0.54$		
			MAX1665X	$V_{B4P} - 1.8$	$V_{B4P} - 0.54$		
DSG Output Voltage High (Note 2)		MAX1665X, $I_{OUT} = 100\mu\text{A}$ , $V_{B4P} = 24V$ , $V_{BN} = 100\text{mV}$			17	20	V
CHG Output Voltage Low	$V_{CHGL}$	$I_{CHG} = -100\mu\text{A}$				$V_{PKN} + 0.1$	V
DSG Output Voltage Low	$V_{DSGL}$	$I_{DSG} = -1\mu\text{A}$				$V_{BN} + 0.1$	V
CHG, DSG Output Source Current	$I_{OH}$	CHG = PKN, DSG = BN		10	25		mA
CHG Output Sink Current	$I_{OL}$	$V_{CHG} = V_{PKN} + 3.0V$		0.5	2		mA
DSG Output Sink Current	$I_{OL}$	$V_{DSG} = V_{BN} + 3.0V$		0.5	2		$\mu\text{A}$
Overcurrent Sampling - $t_{ON}$	$t_{ON}$	$V_{PKN} = \pm 300\text{mV}$			8.2		ms
Overcurrent Sampling - $t_{OFF}$	$t_{OFF}$	$V_{PKN} = \pm 300\text{mV}$			135		ms
Input Bias Current (Note 3)	$I_{BIAS}$	MAX1665SESA, $V_{B1P} = 4V$			3	10	nA
		MAX1665VEESA, $V_{B1P} = 4V$ , $V_{B2P} = 8V$			3	10	
		MAX1665XESA, $V_{B1P} = 4V$ , $V_{B2P} = 8V$ , $V_{B3P} = 12V$			3	10	

# Lithium-Ion Battery Pack Protector

MAX1665S/V/X

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{B2P} = 8V$  (MAX1665S),  $V_{B3P} = 12V$  (MAX1665V),  $V_{B4P} = 16V$  (MAX1665X),  $T_A = 0^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Bias Current Matching	$\Delta I_{BIAS}$	(Notes 3, 4)		$\pm 500$		pA
Supply Current	$I_{CC}$			16	25	$\mu A$
Standby Mode Current	$I_{LP}$	(Note 5)		0.7	1	$\mu A$
Undervoltage Lockout	$V_{UVLO}$	DSG = CHG = low		4.0	4.7	V

## ELECTRICAL CHARACTERISTICS

( $V_{B2P} = 8V$  (MAX1665S),  $V_{B3P} = 12V$  (MAX1665V),  $V_{B4P} = 16V$  (MAX1665X),  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
B2P Voltage Range	$V_{B2P}$	MAX1665S	4		10	V
B3P Voltage Range	$V_{B3P}$	MAX1665V	4		15	V
B4P Voltage Range	$V_{B4P}$	MAX1665X	4		20	V
Overvoltage Threshold	$V_{OV}$	Cell voltage rising	4.20		4.24	V
Undervoltage Threshold	$V_{UV}$		2.4		2.6	V
Undervoltage RESET	$V_{RE}$	$V_{BN} - V_{PKN}$	0		30	mV
Overcurrent Sense Threshold	$V_{CH}$		$\pm 180$		$\pm 320$	mV
CHG, DSG Output Voltage High		$I_{OUT} = 100\mu A$ MAX1665S	$V_{B2P} - 2$	$V_{B2P} - 0.5$		V
		MAX1665V	$V_{B3P} - 2$	$V_{B3P} - 0.5$		
		MAX1665X	$V_{B4P} - 2$	$V_{B4P} - 0.5$		
DSG Output Voltage High (Note 2)		MAX1665X, $I_{OUT} = 100\mu A$ , $V_{B4P} = 24V$ , $V_{BN} = 100mV$			20	V
CHG Output Voltage Low	$V_{CHGL}$	$I_{CHG} = -100\mu A$		$V_{PKN} + 0.1$		V
DSG Output Voltage Low	$V_{DSGL}$	$I_{DSG} = -1\mu A$		$V_{BN} + 0.1$		V
CHG, DSG Output Source Current	$I_{OH}$	CHG = PKN, DSG = BN	10			mA
CHG Output Sink Current	$I_{OL}$	$V_{CHG} = V_{PKN} + 0.3V$	0.2			mA
DSG Output Sink Current	$I_{OL}$	$V_{DSG} = V_{BN} + 0.3V$	0.2			$\mu A$
Input Bias Current (Note 3)	$I_{BIAS}$	MAX1665SESA, $V_{B1P} = 4V$			10	nA
		MAX1665VESA, $V_{B1P} = 4V$ , $V_{B2P} = 8V$			10	
		MAX1665XESA, $V_{B1P} = 4V$ , $V_{B2P} = 8V$ , $V_{B3P} = 12V$			10	
Supply Current	$I_{CC}$				30	$\mu A$
Standby Mode Current	$I_{LP}$	(Note 5)			2	$\mu A$
Undervoltage Lockout	$V_{UVLO}$	DSG = CHG = low			4.7	V

**Note 1:** Applies to the differential voltage measured on any cell.

**Note 2:** DSG is internally clamped to a maximum of 20V to protect the external MOSFET ( $V_{GS}$ ).

**Note 3:** Guaranteed by design.

**Note 4:** The input bias matching between cells is measured with a 4V voltage between cells.

**Note 5:** At least one cell is  $< V_{UV}$ .

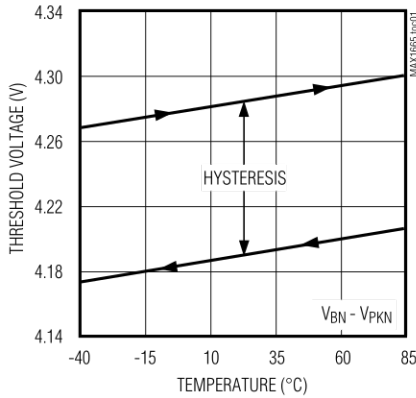
**Note 6:** Specifications to  $-40^{\circ}C$  are guaranteed by design, not production tested.

# Lithium-Ion Battery Pack Protector

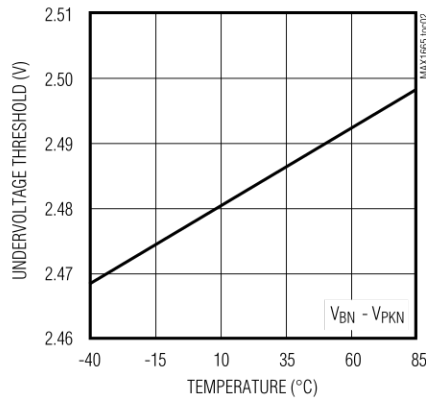
## Typical Operating Characteristics

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

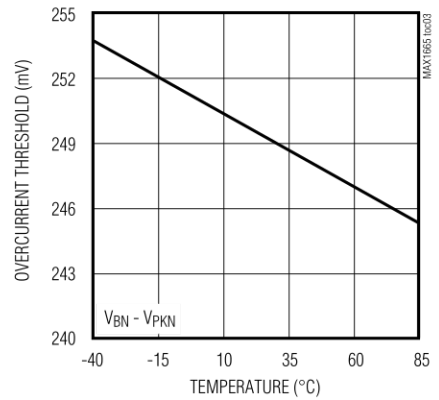
**OVERVOLTAGE THRESHOLD vs. TEMPERATURE**



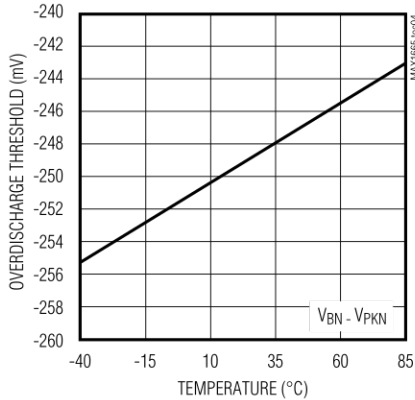
**UNDERVOLTAGE THRESHOLD vs. TEMPERATURE**



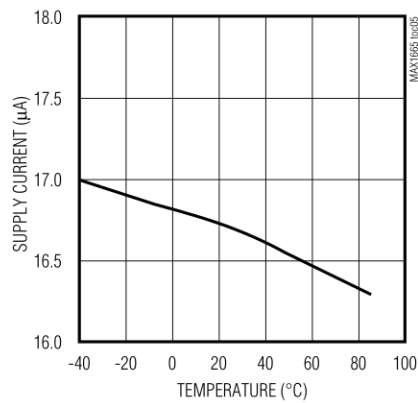
**OVERCURRENT THRESHOLD vs. TEMPERATURE**



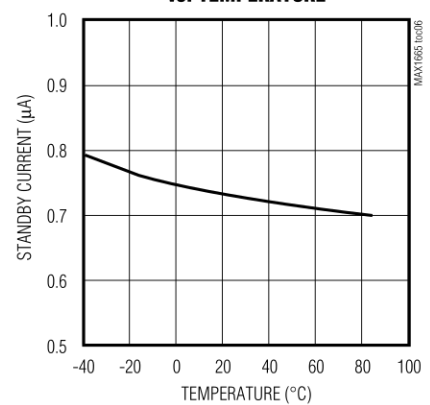
**OVERDISCHARGE THRESHOLD vs. TEMPERATURE**



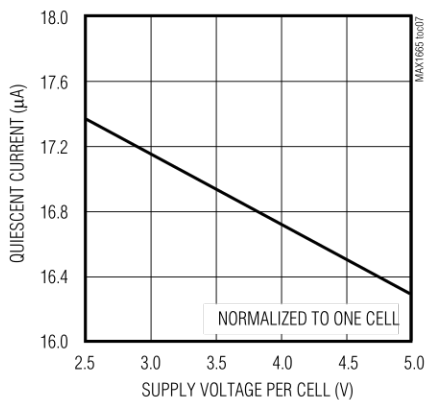
**SUPPLY CURRENT vs. TEMPERATURE**



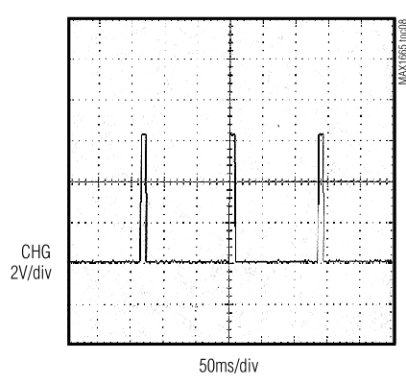
**STANDBY MODE CURRENT vs. TEMPERATURE**



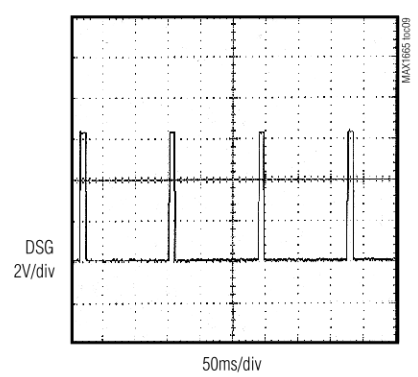
**QUIESCENT CURRENT vs. SUPPLY VOLTAGE**



**CONTINUOUS OVERCHARGE CONDITION**



**CONTINUOUS OVERDISCHARGE CONDITION**



# Lithium-Ion Battery Pack Protector

## Pin Description

**MAX1665S/V/X**

PIN			NAME	FUNCTION
MAX1665S	MAX1665V	MAX1665X		
1, 8	1	—	I.C.	Internally Connected. Make no connection to this pin.
—	—	1	B4P	Cell 4 Positive Input. Connect to the positive terminal of the fourth series Li+ cell.
2	2	2	DSG	Discharge Control Output. Drives the gate of an external N-channel MOSFET to control the discharge path.
3	3	3	CHG	Charge Control Output. Drives the gate of an external N-channel MOSFET to control the charge path.
4	4	4	PKN	Pack Negative Input
5	5	5	BN	Connect to the negative terminal of the first series Li+ cell.
6	6	6	B1P	Cell 1 Positive Input. Connect to the positive terminal of the first series Li+ cell.
7	7	7	B2P	Cell 2 Positive Input. Connect to the positive terminal of the second series Li+ cell.
—	8	8	B3P	Cell 3 Positive Input. Connect to the positive terminal of the third series Li+ cell.

**Table 1. Functionality Truth Table for  $V_{BN} < V_{PKN} + 0.018V$  (Discharge Mode)**

CHARGE OVERCURRENT	DISCHARGE OVERCURRENT	OVERVOLTAGE	UNDERVOLTAGE	CHG	DSG	GATE CLOCKED	MAX SUPPLY CURRENT* ( $\mu A$ )
0	0	0	0	High	High	No	25
0	0	0	1	Low	Low	No	1
0	0	1	0	Low	High	No	25
0	0	1	1	Low	Low	No	1
0	1	0	0	Gated	Gated	Yes	25
0	1	0	1	Low	Low	No	1
0	1	1	0	Low	Gated	Yes	25
0	1	1	1	Low	Low	No	1

\*Assuming no load on CHG or DSG.

**MAX1665S/V/X**

**Table 2. Functionality Truth Table for  $V_{BN} > V_{PKN} + 0.018V$  (Charge Mode)**

CHARGE OVERCURRENT	DISCHARGE OVERCURRENT	OVERVOLTAGE	UNDERVOLTAGE	CHG	DSG	GATE CLOCKED	MAX SUPPLY CURRENT (μA)
0	0	0	0	High	High	No	25
0	0	0	1	High	High	No	25
0	0	1	0	Low	High	No	25
0	0	1	1	Low	High	No	25
1	0	0	0	Gated	Gated	Yes	25
1	0	0	1	Gated	Gated	Yes	25
1	0	1	0	Low	High	No	25
1	0	1	1	Low	High	No	25

\*Assuming no load on CHG or DSG.

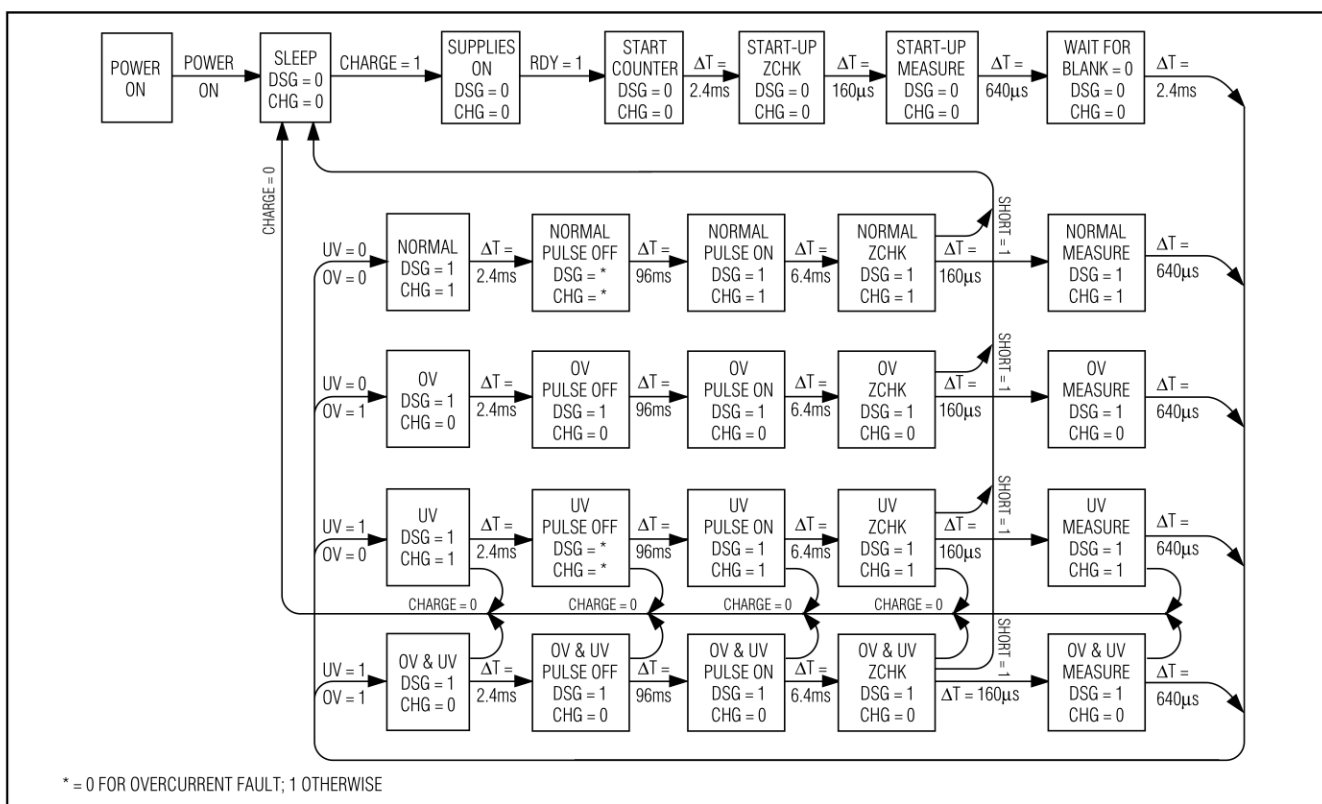


Figure 1. State Diagram

### ***Detailed Description***

The MAX1665S, MAX1665V, and MAX1665X supervise the charging and discharging processes on Li+ cells. Designed for 2, 3, and 4-cell applications, these devices monitor the voltage across each cell to provide protection against overcurrent, overvoltage, and undervoltage.

Figure 1 shows the MAX1665 state diagram. Two control pins, CHG and DSG, drive the gates of two series-connected external N-channel MOSFETs, enabling/disabling the charging/discharging process as necessary (see *Typical Operating Circuit*). The voltages at B1P, B2P, B3P, and B4P are measured differentially

# Lithium-Ion Battery Pack Protector

across each cell to determine if the voltage levels are within operating range.

As depicted in the typical operating circuit, when CHG and DSG are high, the MOSFETs are on, allowing the cells to charge or discharge. However, when the charge or discharge current becomes excessive, the device turns off the FETs, enters a standby mode, and periodically samples the current to determine if the fault condition is removed. The MAX1665 does not sample the current directly, but rather measures the differential voltage across BN and PKN produced by the charge or discharge current flowing through the drain-to-source resistance of the MOSFETs. A preset voltage threshold is used to prevent excess current flow (see *Electrical Characteristics*).

In operating mode, all of the MAX1665 versions consume less than 25µA of quiescent current, allowing long-term battery storage without significantly affecting battery life. In standby mode, these devices consume less than 1µA of quiescent current.

## Overvoltage Protection

When any individual cell voltage rises above  $V_{OV}$  (over-voltage limit), the charge MOSFET control pin (CHG) is driven to PKN, thereby disconnecting the charger from the cells. The MAX1665 measures each cell of the pack differentially to prevent overcharging on a cell-by-cell basis. The charging process resumes when the highest cell voltage drops below  $V_{OV} - 100\text{mV}$  (see *Typical Operating Circuit*).

## Undervoltage/Overdischarge Protection

Discharge can occur whenever the voltage of each cell is above the undervoltage threshold voltage ( $V_{UV}$ , typically 2.50V). If the voltage on any of the cells falls below  $V_{UV}$ , CHG latches to PKN and DSG latches to BN. Quiescent current falls to under 1µA as the device enters the standby mode. The latch resets when BN exceeds PKN by 18mV.

During charge mode, when BN is greater than PKN, the latch is held in reset, which disables the undervoltage comparator feature and allows charging on the cells. During the initialization process, as cells are connected to the MAX1665, the device considers this a low-voltage condition and disables CHG and DSG until a charging source is applied to create at least an 18mV differential between BN and PKN.

During long-term storage, the battery will self-discharge until it reaches the undervoltage threshold. When this happens, the MAX1665 enters standby mode. Normal operating mode resumes when a charger is connected, causing BN to rise 18mV above PKN.

## Overcurrent Protection

When the MAX1665 detects overcurrent in the system, it disables the charge or discharge process by connecting CHG to PKN and DSG to BN, turning off the external MOSFETs (see *Typical Operating Circuit*). In charge mode, the MAX1665 detects overcharge when the voltage from BN to PKN exceeds +250mV. In discharge mode, overdischarge occurs when the differential voltage is less than -250mV. During any overcurrent condition, CHG and DSG are gated at 12Hz until the overcurrent is removed.

If both an overvoltage and overcharge condition exist, the overvoltage condition takes priority. Likewise, if undervoltage and overdischarge conditions exist, the overdischarge condition takes priority. For more details, see Tables 1 and 2.

## Cell Current Balancing

When the battery cells are matched, the MAX1665 draws zero current from the intermediate nodes. The MAX1665 draws current from the top terminal only. Figure 2 shows a simplified diagram of the voltage sampling scheme. The following equations show that, for balanced cells, the differential discharge currents are zero:

$$\text{B4P: } I_4 = 3I_{CB} + V_4 / R = 4V_4 / R = \text{BAT4 current}$$

$$\text{B3P: } I_3 = I_3P + I_4 = \text{BAT3 current}$$

$$I_3P + I_{CB} = V_3 / R \Rightarrow I_3P = V_3 / R - V_4 / R$$

$$I_3 = I_4 + (V_3 - V_4) / R = (3V_4 + V_3) / R$$

$$\text{B2P: } I_2 = I_2P + I_3 = \text{BAT2 current}$$

$$I_2P + I_{CB} = V_2 / R \Rightarrow I_2P = V_2 / R - V_4 / R$$

$$I_2 = I_3 + V_2 / R - V_4 / R = I_4 + (V_3 - V_4) / R + (V_2 - V_4) / R = (2V_4 + V_3 + V_2) / R$$

$$\text{B1P: } I_1 = I_1P + I_2 = \text{BAT1 current}$$

$$I_1P + I_{CB} = V_1 / R \Rightarrow I_1P = V_1 / R - V_4 / R$$

$$I_1 = I_2 + V_1 / R - V_4 / R = I_4 + (V_3 - V_4) / R + (V_2 - V_4) / R + (V_1 - V_4) / R = (V_4 + V_3 + V_2 + V_1) / R$$

$$\text{when } V_1 = V_2 = V_3 = V_4, I_1P = I_2P = I_3P = 0 \text{ and } I_1 = I_2 = I_3 = I_4 = 4V_4 / R.$$

Due to process variations, the MAX1665 does draw a minute current (70nA ~ 150nA) from the intermediate node even when the cells are matched. This current difference exists in the sampling mode, which is 1/32 of the whole time period, making the average of this current 2nA to 5nA.

# Lithium-Ion Battery Pack Protector

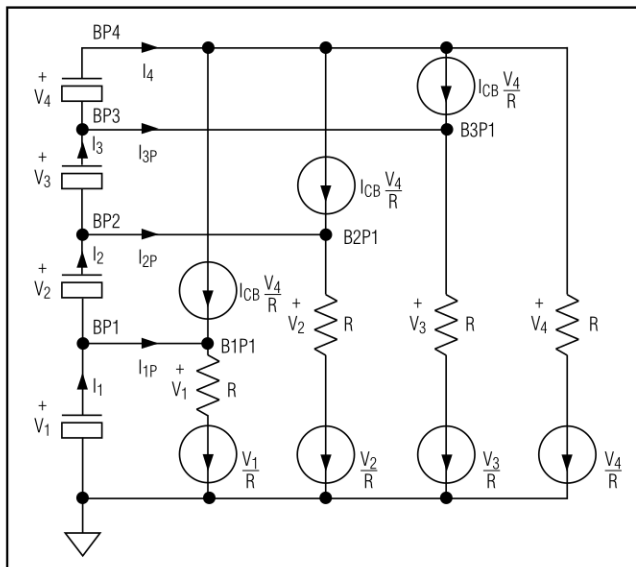


Figure 2. Sampling Mode Equivalent Circuit

## Applications Information

### Choosing an External MOSFET

The external N-channel MOSFETs act as gated switches to enable or disable the charging/discharging process. CHG and DSG control the gate of these external MOSFETs to prevent damage to the Li+ cells. For overcurrent conditions, the voltage at DSG equals the voltage at BN, thereby reducing all current flow, including the path through the body diode of the N-channel MOSFET. Note that the MAX1665X clamps the V<sub>GS</sub> voltage to a maximum of 20V.

The IRF7101 is a low-cost, dual N-channel MOSFET that is available in a small 8-pin SO package. Depending on the maximum charge and discharge rates, use different MOSFETs to optimize each application. Table 3 summarizes recommended MOSFETs.

### 2, 3, and 4-Cell Applications

Figures 3 through 5 depict circuits for 2, 3, and 4-cell applications. Note that the two series MOSFETs (IRF7101 dual N-channel MOSFETs) are oriented to prevent body diode current flow. The indicated polarity symbols show the connection for the external source required to charge the Li+ cells. This external charger source also supplies the gate drive to the MOSFETs through pack + voltage / pack.

Table 3. Recommended MOSFETs

DUAL N-CHANNEL MOSFETs	TYPICAL R <sub>DS(ON)</sub> (Ω)	MAX V <sub>GS</sub> (V)
IRF9956	0.10	±20
FDS6990A	0.018	±20
Si9936	0.050	±20

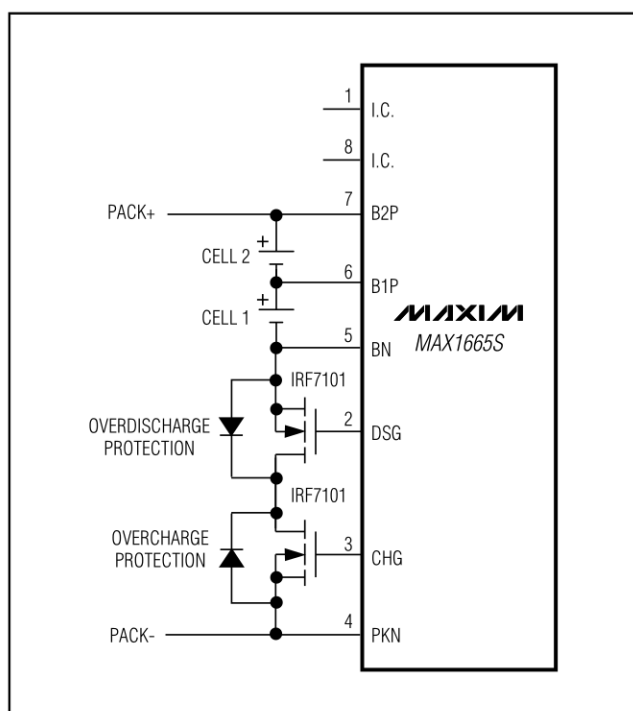


Figure 3. Typical 2-Cell Operating Circuit

# Lithium-Ion Battery Pack Protector

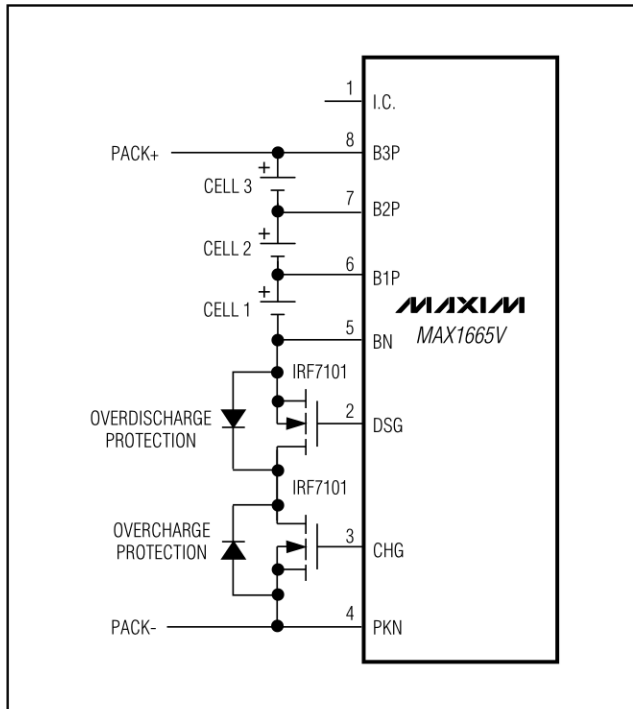


Figure 4. Typical 3-Cell Operating Circuit

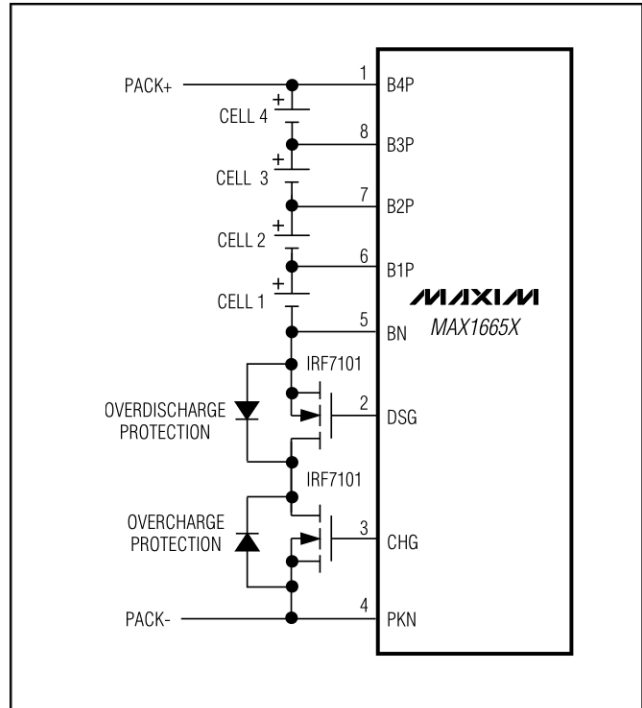
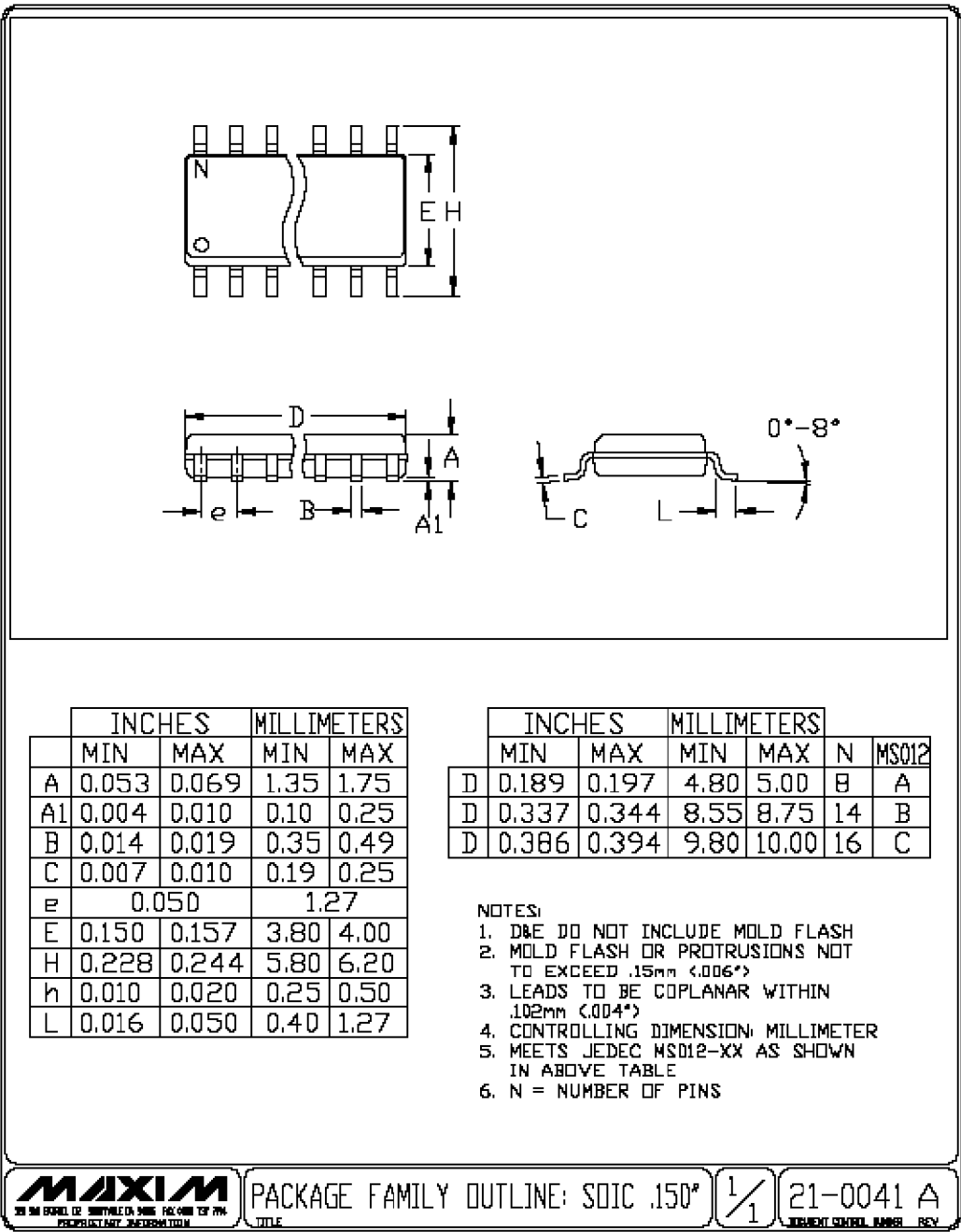


Figure 5. Typical 4-Cell Operating Circuit

MAX1665S/V/X

# Lithium-Ion Battery Pack Protector

## Package Information



# ***Lithium-Ion Battery Pack Protector***

NOTES

**MAX1665S/V/X**

# ***Lithium-Ion Battery Pack Protector***

## **NOTES**

*Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.*

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