MIC4426/7/8

Dual 1.5A-Peak Low-Side MOSFET Drivers

Features

- Bipolar/CMOS/DMOS Construction
- Latch-Up Protected to >500 mA Reverse Current
- 1.5A-Peak Output Current
- 4.5V to 18V Operating Range
- Low Quiescent Supply Current
  - 4 mA at Logic 1 Input
  - 400 µA at Logic 0 Input
- Switches 1000 pF in 25 ns
- Matched Rise and Fall Times
- 7Ω Output Impedance
- <40 ns Typical Delay
- Logic-Input Threshold Independent of Supply Voltage
- Logic-Input Protection to –5V
- 6 pF Typical Equivalent Input Capacitance
- 25 mV Max. Output Offset from Supply or Ground
- Replaces MIC426/7/8 and MIC1426/7/8
- Dual inverting, dual non-inverting, and inverting/non-inverting configurations
- ESD Protection

Applications

- MOSFET Driver
- Clock Line Driver
- Coax Cable Driver
- Piezoelectric Transducer Driver

General Description

The MIC4426/4427/4428 family are highly reliable dual low-side MOSFET drivers fabricated on a BiCMOS/DMOS process for low power consumption and high efficiency. These drivers translate TTL or CMOS input logic levels to output voltage levels that swing within 25 mV of the positive supply or ground. Comparable bipolar devices are capable of swinging only to within 1V of the supply. The MIC4426/7/8 is available in three configurations: dual inverting, dual non-inverting, and one inverting plus one non-inverting output.

The MIC4426/4427/4428 are pin-compatible replacements for the MIC426/427/428 and MIC1426/1427/1428 with improved electrical performance and rugged design. They can withstand up to 500 mA of reverse current (either polarity) without latching and up to 5V noise spikes (either polarity) on ground pins.

Primarily intended for driving power MOSFETs, MIC4426/7/8 drivers are suitable for driving other loads (capacitive, resistive, or inductive) that require low-impedance, high peak current, and fast switching time. Other applications include driving heavily loaded clock lines, coaxial cables, or piezoelectric transducers. The only load limitation is that total driver power dissipation must not exceed the limits of the package.

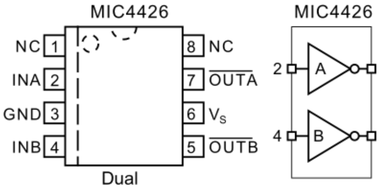
See MIC4126/4127/4128 for high power and narrow pulse applications.

Package Types

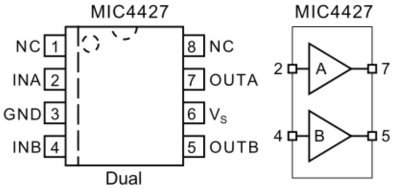
MIC4426
SOIC-8 (M)
MSOP-8 (MM)
PDIP-8 (N)
(Top View)

MIC4427
SOIC-8 (M)
MSOP-8 (MM)
PDIP-8 (N)
(Top View)

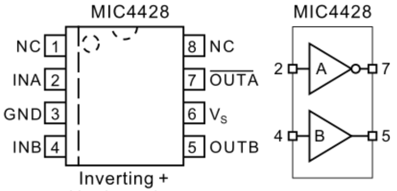
MIC4428
SOIC-8 (M)
MSOP-8 (MM)
PDIP-8 (N)
(Top View)



Dual
Inverting

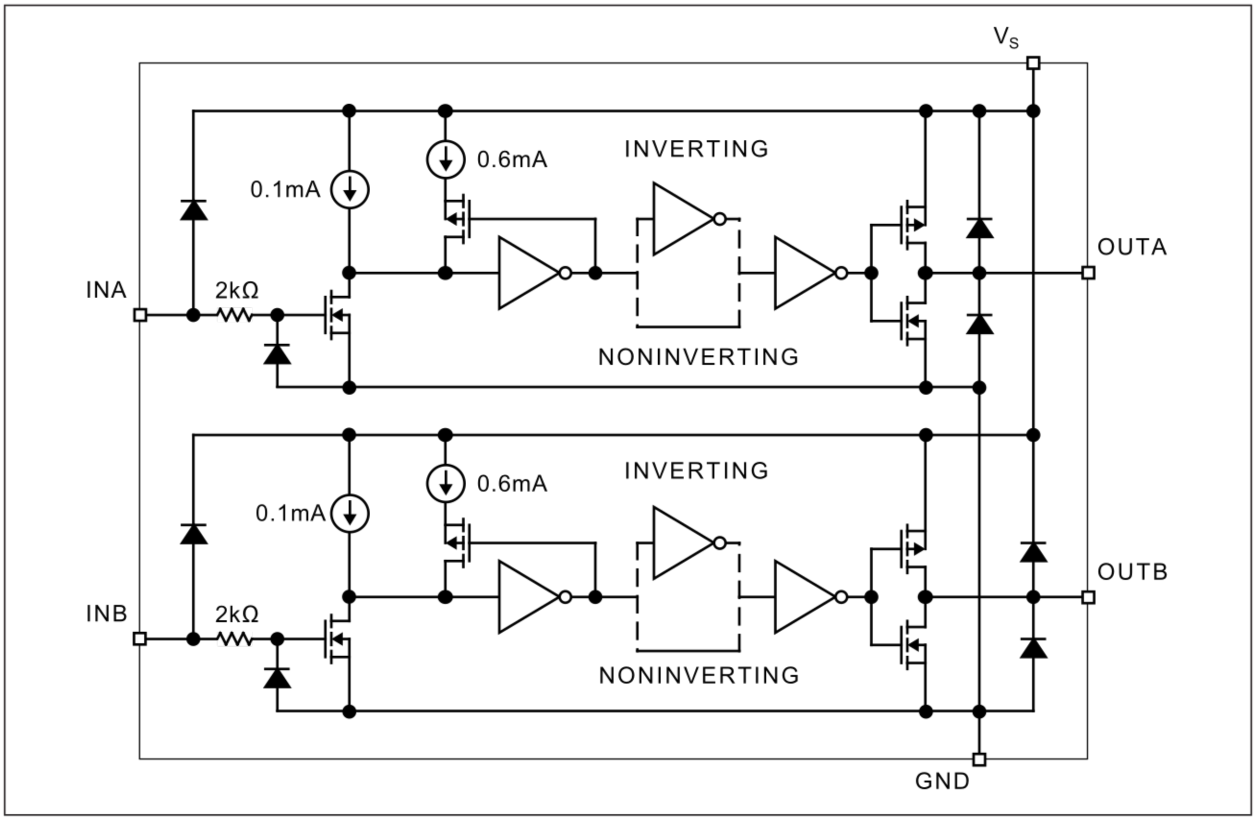


Dual
Noninverting



Inverting +
Noninverting

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_S) .... +22V
Input Voltage (V_{IN}) .... V_S + 0.3V to GND – 5V
ESD Rating .... (Note 1)

Operating Ratings ††

Supply Voltage (V_S) .... +4.5V to +18V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions are recommended.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: 4.5V ≤ V_S ≤ 18V; T_A = +25°C, **bold** values valid for full specified temperature range; unless noted. Note 1

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Input						
Logic 1 Input Voltage	V_{IH}	2.4	1.4	—	V	—
		2.4	**1.5**	—		
Logic 0 Input Voltage	V_{IL}	—	1.1	0.8	V	—
		—	**1.0**	**0.8**		
Input Current	I_{IN}	**–1**	—	**1**	µA	0V ≤ V_{IN} ≤ V_S
Output						
High Output Voltage	V_{OH}	**V_S – 0.025**	—	—	V	—
Low Output Voltage	V_{OL}	—	—	**0.025**	V	—
Output Resistance	R_O	—	6	10	Ω	I_{OUT} = 10 mA, V_S = 18V
		—	**8**	**12**		
Peak Output Current	I_{PK}	—	**1.5**	—	A	—
Latch-Up Protection	I	**>500**	—	—	mA	Withstand Reverse Current
Switching Time						
Rise Time	t_r	—	18	30	ns	Test Figure 1-1
		—	**20**	**40**		—
Fall Time	t_f	—	15	20	ns	Test Figure 1-1
		—	**29**	**40**		—
Delay Time	t_{D1}	—	17	30	ns	Test Figure 1-1
		—	**19**	**40**		—
Delay Time	t_{D2}	—	23	50	ns	Test Figure 1-1
		—	**27**	**60**		—

Note 1: Specification for packaged product only.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: 4.5V ≤ V_S ≤ 18V; T_A = +25°C, **bold** values valid for full specified temperature range; unless noted. Note 1

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Pulse Width	t_{PW}	**400**	—	—	ns	Test Figure 1-1
Power Supply						
Power Supply Current	I_S	0.6	1.4	4.5	mA	$V_{INA} = V_{INB} = 3.0V$
		—	**1.5**	**8**		—
Power Supply Current	I_S	—	0.18	0.4	mA	$V_{INA} = V_{INB} = 0V$
		—	**0.19**	**0.6**		—

Note 1: Specification for packaged product only.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Maximum Junction Temperature	T_J	—	—	+150	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	—	—	—	+300	°C	10 sec.
Junction Operating Temperature Range	T_J	0	—	+70	°C	Z option
Junction Operating Temperature Range	T_J	–40	—	+85	°C	Y option
Package Thermal Resistances						
Thermal Resistance, PDIP 8-Ld	θ_{JA}	—	130	—	°C/W	—
Thermal Resistance, PDIP 8-Ld	θ_{JC}	—	42	—	°C/W	—
Thermal Resistance, SOIC 8-Ld	θ_{JA}	—	120	—	°C/W	—
Thermal Resistance, SOIC 8-Ld	θ_{JC}	—	75	—	°C/W	—
Thermal Resistance, MSOP 8-Ld	θ_{JA}	—	250	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

Test Circuits

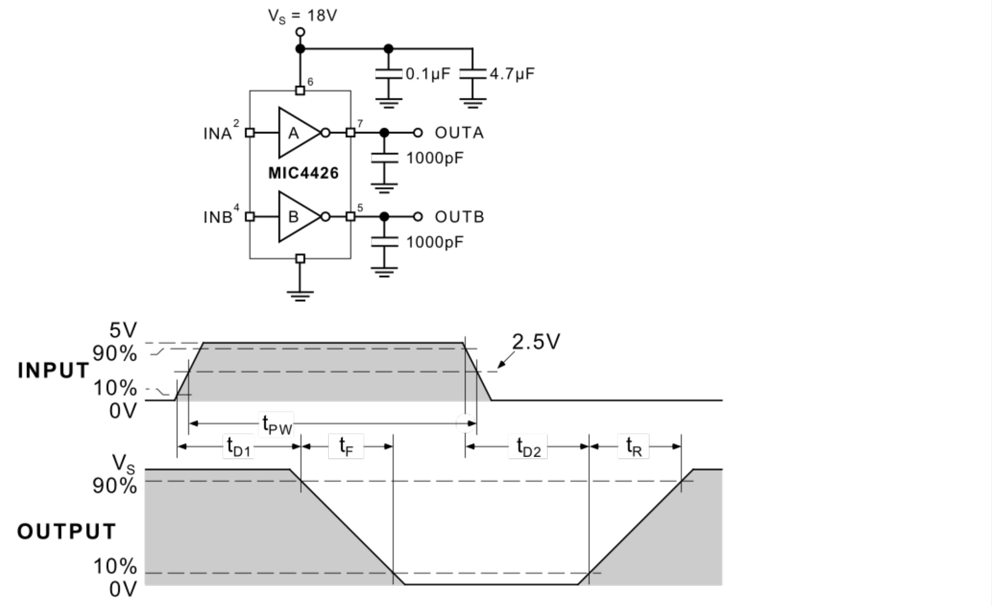


FIGURE 1-1: *Inverting Driver Switching Time.*

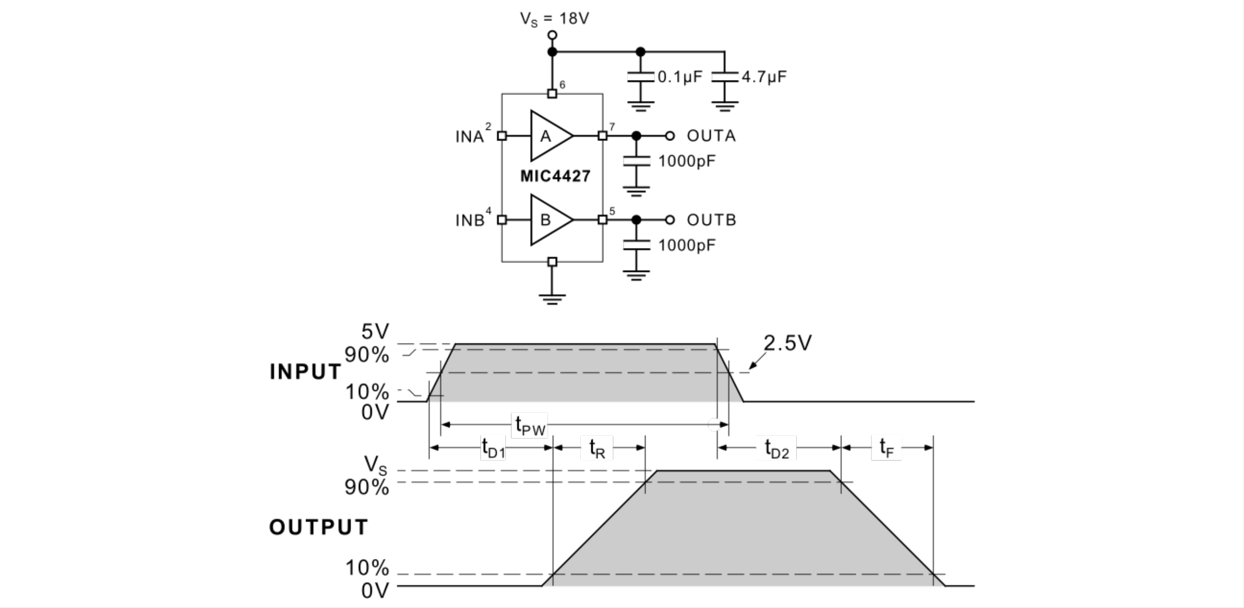


FIGURE 1-2: *Non-Inverting Driver Switching Time.*

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

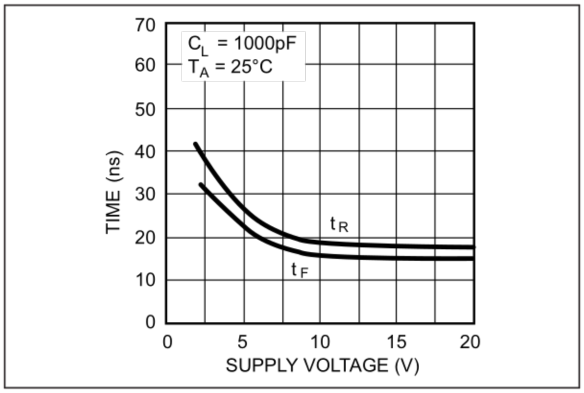


FIGURE 2-1: *Rise and Fall Time vs. Supply Voltage.*

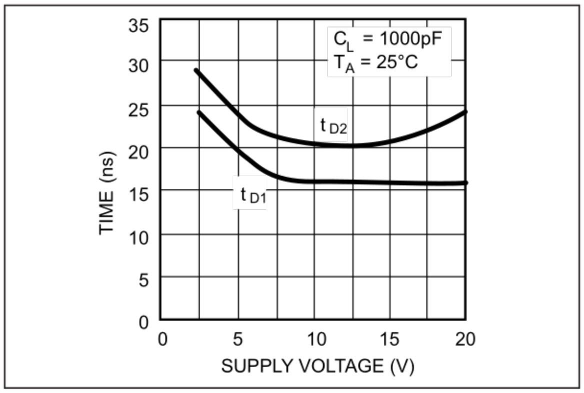


FIGURE 2-2: *Delay Time vs. Supply Voltage.*

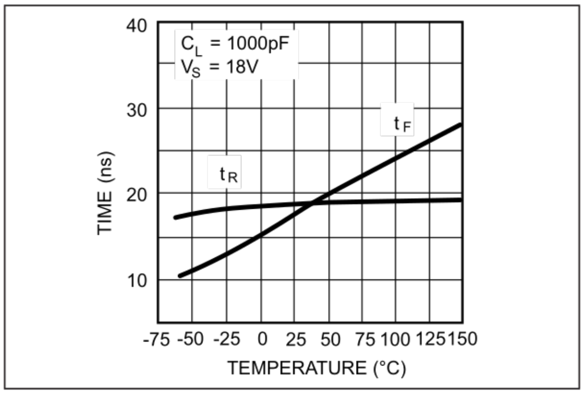


FIGURE 2-3: *Rise and Fall Time vs. Temperature.*

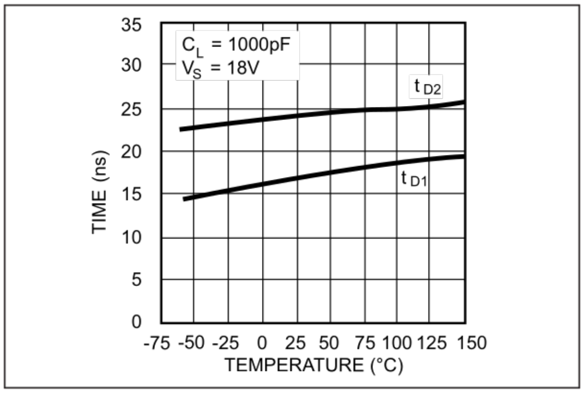


FIGURE 2-4: *Delay Time vs. Temperature.*

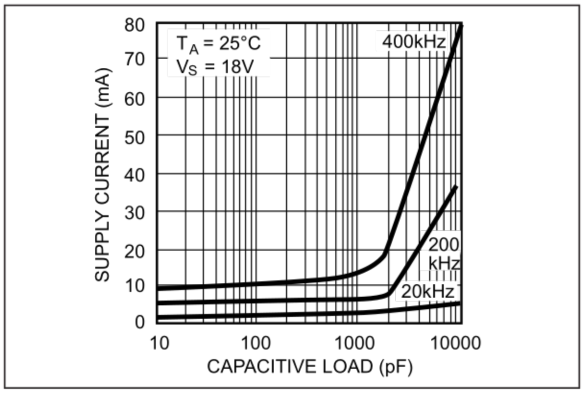


FIGURE 2-5: *Supply Current vs. Capacitive Load.*

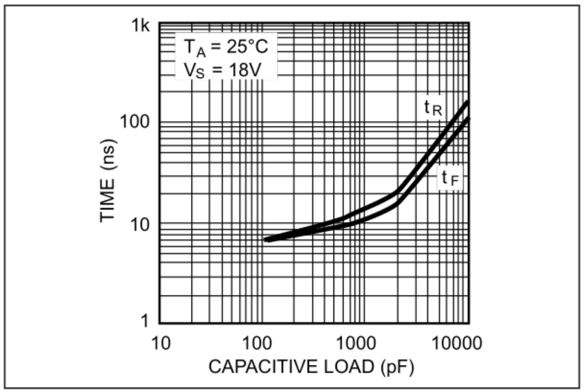


FIGURE 2-6: *Rise and Fall Time vs. Capacitive Load.*

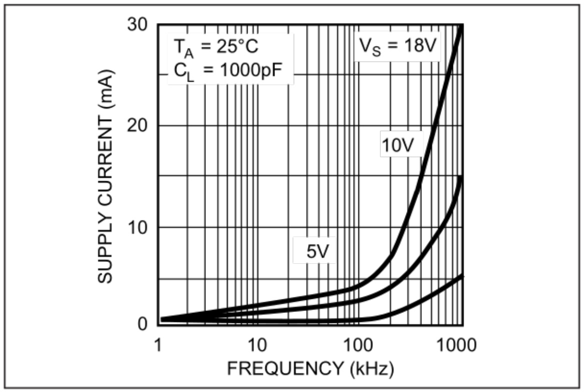


FIGURE 2-7: *Supply Current vs. Frequency.*

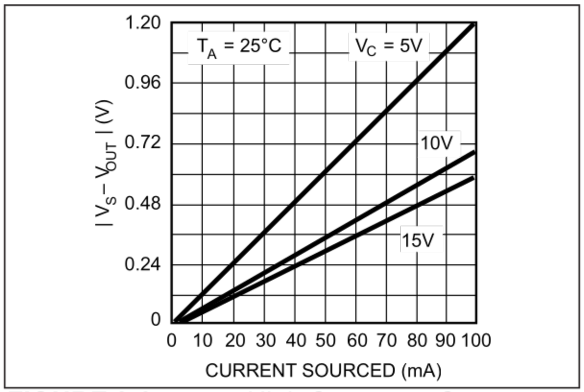


FIGURE 2-8: *High Output vs. Current.*

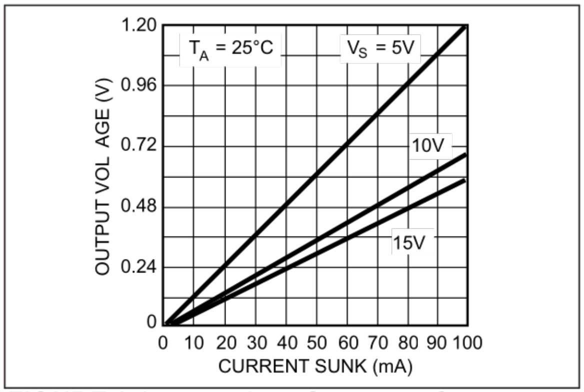


FIGURE 2-9: *Low Output vs. Current.*

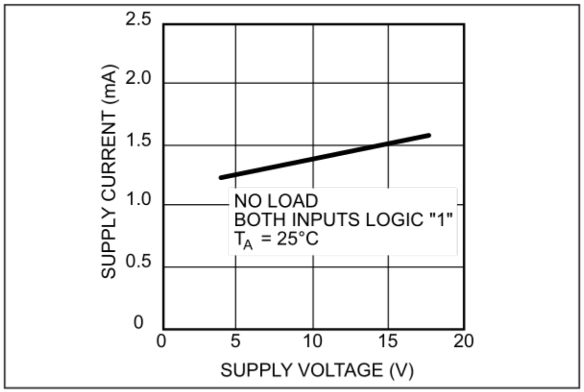


FIGURE 2-10: *Quiescent Power Supply Current vs. Supply Voltage.*

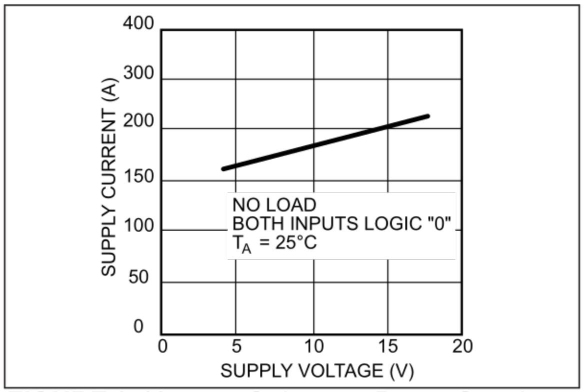


FIGURE 2-11: *Quiescent Power Supply Current vs. Supply Voltage.*

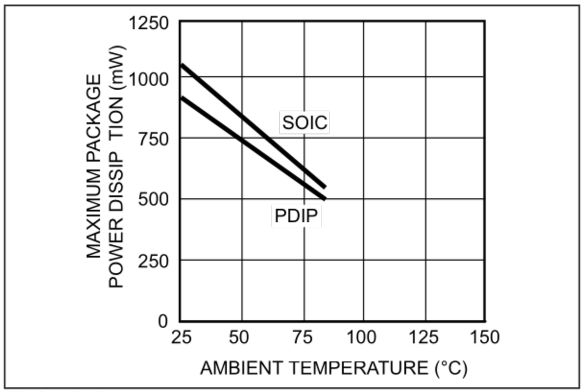


FIGURE 2-12: *Package Power Dissipation.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1, 8	NC	Not internally connected.
2	INA	Control Input A: TTL/CMOS compatible logic input.
3	GND	Ground.
4	INB	Control Input B: TTL/CMOS compatible logic input.
5	OUTB	Output B: CMOS totem-pole output.
6	VS	Supply Input: +4.5V to +18V.
7	OUTA	Output A: CMOS totem-pole output.

4.0 APPLICATION INFORMATION

4.1 Supply Bypassing

Large currents are required to charge and discharge large capacitive loads quickly. For example, changing a 1000 pF load by 16V in 25 ns requires 0.8A from the supply input.

To guarantee low supply impedance over a wide frequency range, parallel capacitors are recommended for power supply bypassing. Low-inductance ceramic MLC capacitors with short lead lengths (< 0.5”) should be used. A 1.0 µF film capacitor in parallel with one or two 0.1 µF ceramic MLC capacitors normally provides adequate bypassing.

4.2 Grounding

When using the inverting drivers in the MIC4426 or MIC4428, individual ground returns for the input and output circuits or a ground plane are recommended for optimum switching speed. The voltage drop that occurs between the driver’s ground and the input signal ground, during normal high-current switching, will behave as negative feedback and degrade switching speed.

4.3 Control Input

Unused driver inputs must be connected to logic high (which can be VS) or ground. For the lowest quiescent current (<500 µA), connect unused inputs to ground. A logic high signal will cause the driver to draw up to 9 mA.

The drivers are designed with 100 mV of control input hysteresis. This provides clean transitions and minimizes output stage current spikes when changing states. The control input voltage threshold is approximately 1.5V. The control input recognizes 1.5V up to VS as a logic high and draws less than 1 µA within this range.

The MIC4426/7/8 drives the TL494, SG1526/7, MIC38C42, TSC170, and similar switch-mode power supply integrated circuits.

4.4 Power Dissipation

Power dissipation should be calculated to make sure that the driver is not operated beyond its thermal ratings. Quiescent power dissipation is negligible. A practical value for total power dissipation is the sum of the dissipation caused by the load and the transition power dissipation ($P_L + P_T$).

4.5 Load Dissipation

Power dissipation caused by continuous load current (when driving a resistive load) through the driver’s output resistance is:

EQUATION 4-1:

$$P_L = I_L^2 \times R_O$$

For capacitive loads, the dissipation in the driver is:

EQUATION 4-2:

$$P_L = f \times C_L \times V_S^2$$

4.6 Power Dissipation

In applications switching at a high frequency, transition power dissipation can be significant. This occurs during switching transitions when the P-channel and N-channel output FETs are both conducting for the brief moment when one is turning on and the other is turning off.

EQUATION 4-3:

$$P_T = 2 \times f \times V_S \times Q$$

Charge (Q) is read from the following graph:

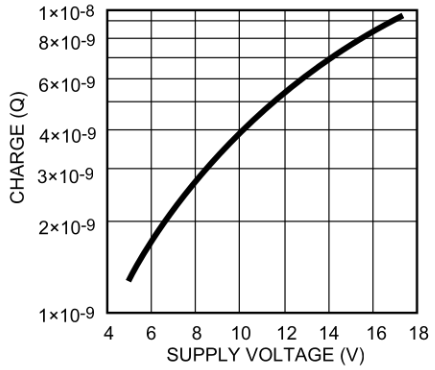
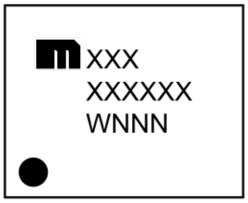


FIGURE 4-1: *Crossover Energy Loss per Transition.*

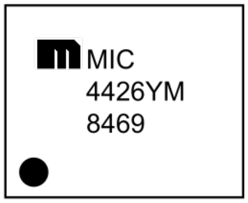
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

8-Lead SOIC*

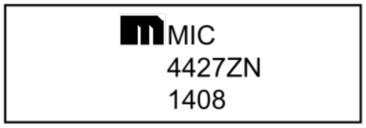


Example

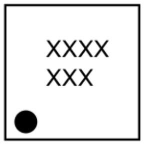


8-Lead PDIP*

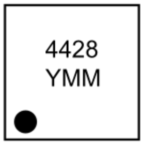
Example



8-Lead MSOP*



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

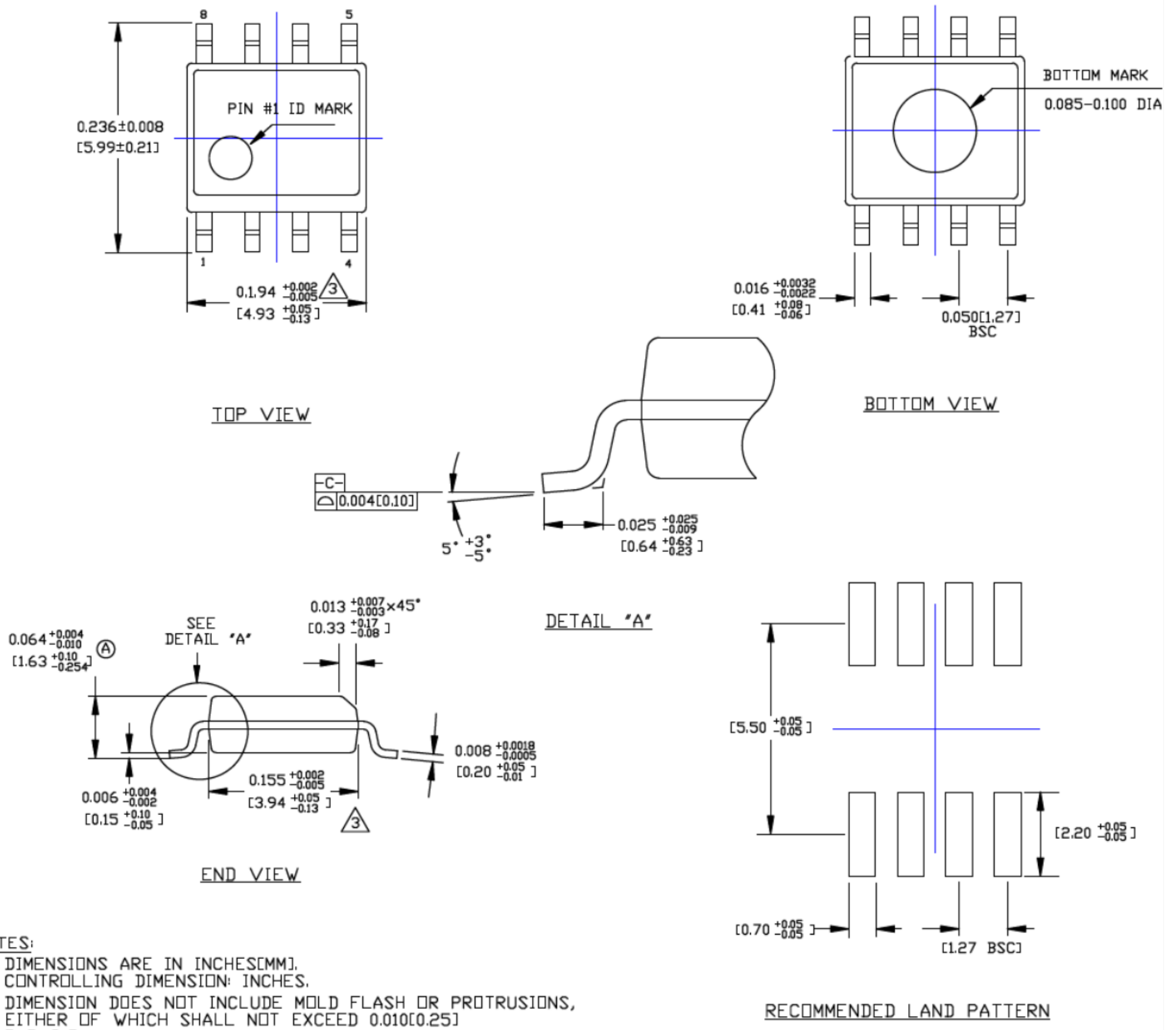
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

8-Lead SOICN Package Outline & Recommended Land Pattern

TITLE
8 LEAD SOICN PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	SOICN-8LD-PL-1	**UNIT**	INCH [MM]



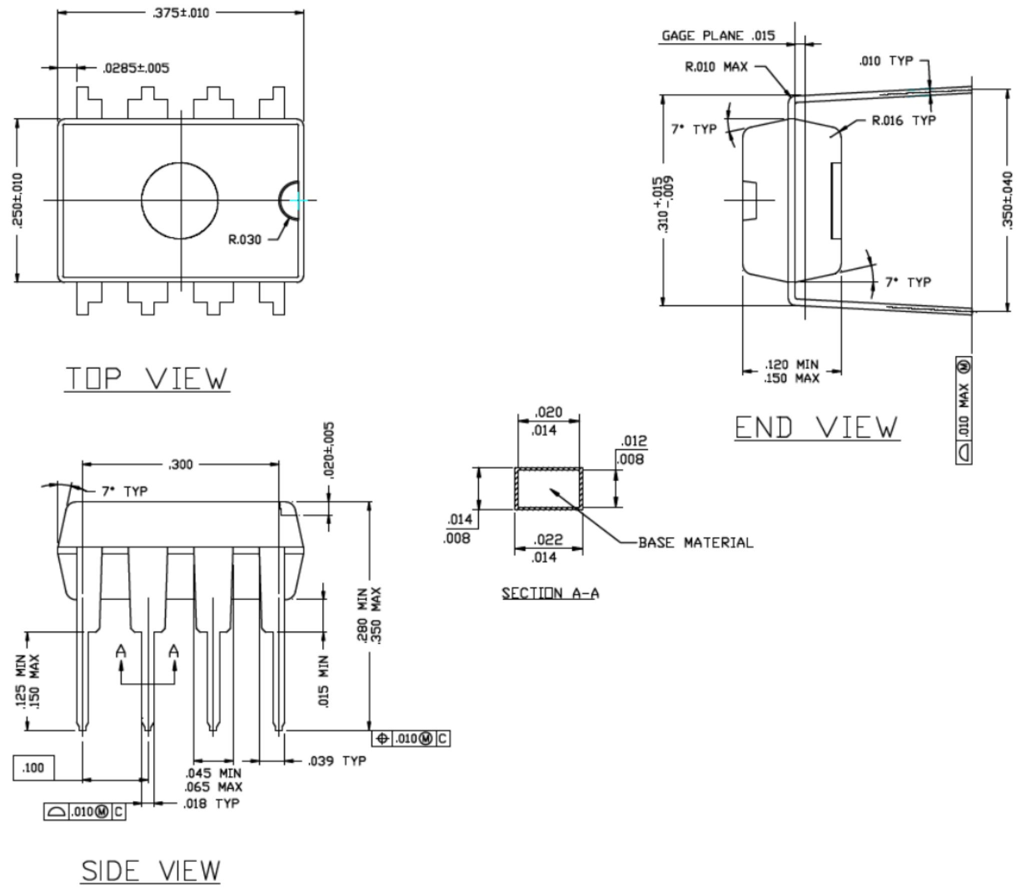
NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.010[0.25] PER SIDE.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

8-Lead PDIP Package Outline and Recommended Land Pattern

TITLE
8 LEAD PDIP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	PDIP-8LD-PL-1	**UNIT**	INCH
Lead Frame	Copper	**Lead Finish**	Matte Tin

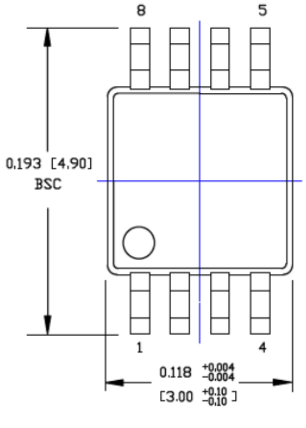


Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

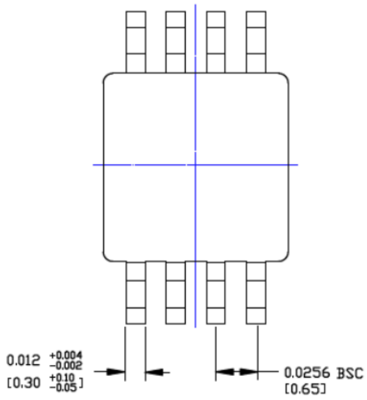
8-Lead MSOP Package Outline and Recommended Land Pattern

TITLE
8 LEAD MSOP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

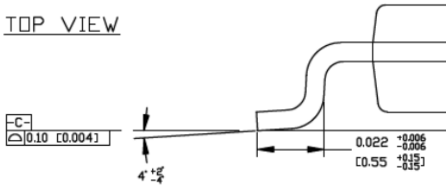
DRAWING #	MSOP-8LD-PL-1	**UNIT**	INCH [MM]



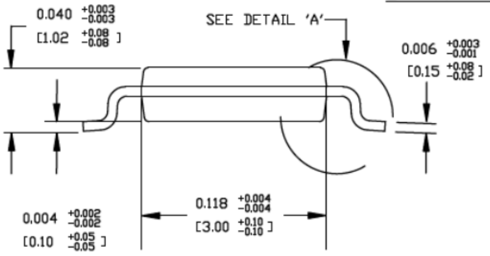
TOP VIEW



BOTTOM VIEW

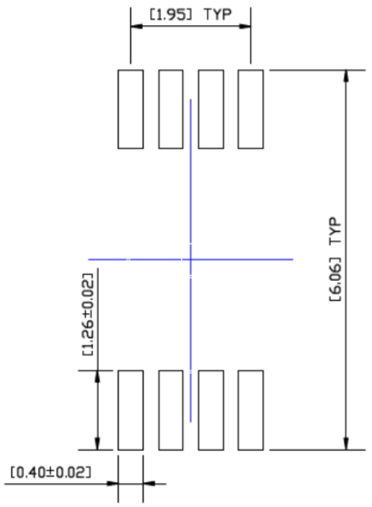


DETAIL A



SIDE VIEW

NOTES:
1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.20] PER SIDE.



RECOMMENDED LAND PATTERN

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (May 2019)

- Converted Micrel document MIC4426/7/8 to Microchip data sheet template DS20006202A.
- Minor grammatical text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Device	**X**	**XX**	**-XX**
Part No.	Junction Temp. Range	Package	Media Type

Device:

MIC4426: Dual Inverting, Dual 1.5A-Peak Low-Side MOSFET Driver
MIC4427: Dual Non-Inverting, Dual 1.5A-Peak Low-Side MOSFET Driver
MIC4428: Inverting and Non-Inverting, Dual 1.5A-Peak Low-Side MOSFET Driver

Junction Temperature Range:

Y = –40°C to +85°C, RoHS-Compliant
Z = 0°C to +70°C, RoHS-Compliant

Package:

N = 8-Lead PDIP
M = 8-Lead SOIC
MM = 8-Lead MSOP

Media Type:

<blank>= 95/Tube (SOIC only)
<blank>= 100/Tube (MSOP only)
<blank>= 50/Tube (PDIP only)
TR = 2,500/Reel (SOIC only)

Examples:

a) MIC4426: Dual Inverting, Dual 1.5A-Peak Low-Side MOSFET Driver, –40°C to +85°C Temp. Range

MIC4426YM	8-Lead SOIC	95/Tube
MIC4426YM-TR	8-Lead SOIC	2,500/Reel
MIC4426YN	8-Lead PDIP	50/Tube
MIC4426YMM	8-Lead MSOP	100/Tube
MIC4426YMM-TR	8-Lead MSOP	2,500/Reel

b) MIC4426: Dual Inverting, Dual 1.5A-Peak Low-Side MOSFET Driver, 0°C to +70°C Temp. Range

MIC4426ZN	8-Lead PDIP	50/Tube
MIC4426ZM	8-Lead SOIC	95/Tube
MIC4426ZM-TR	8-Lead SOIC	2,500/Reel

c) MIC4427: Dual Non-Inverting, Dual 1.5A-Peak Low-Side MOSFET Driver, –40°C to +85°C Temp. Range

MIC4427YM	8-Lead SOIC	95/Tube
MIC4427YM-TR	8-Lead SOIC	2,500/Reel
MIC4427YN	8-Lead PDIP	50/Tube
MIC4427YMM	8-Lead MSOP	100/Tube
MIC4427YMM-TR	8-Lead MSOP	2,500/Reel

d) MIC4427: Dual Non-Inverting, Dual 1.5A-Peak Low-Side MOSFET Driver, 0°C to +70°C Temp. Range

MIC4427ZN	8-Lead PDIP	50/Tube
MIC4427ZM	8-Lead SOIC	95/Tube
MIC4427ZM-TR	8-Lead SOIC	2,500/Reel

e) MIC4428: Inverting + Non-Inverting, Dual 1.5A-Peak Low-Side MOSFET Driver, –40°C to +85°C Temp. Range

MIC4428YM	8-Lead SOIC	95/Tube
MIC4428YM-TR	8-Lead SOIC	2,500/Reel
MIC4428YN	8-Lead PDIP	50/Tube
MIC4428YMM	8-Lead MSOP	100/Tube
MIC4428YMM-TR	8-Lead MSOP	2,500/Reel

f) MIC4428: Inverting + Non-Inverting, Dual 1.5A-Peak Low-Side MOSFET Driver, 0°C to +70°C Temp. Range

MIC4428ZN	8-Lead PDIP	50/Tube
MIC4428ZM	8-Lead SOIC	95/Tube
MIC4428ZM-TR	8-Lead SOIC	2,500/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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