NPN - 2N6515, 2N6517;
PNP - 2N6520

High Voltage Transistors
NPN and PNP

Features

- Voltage and Current are Negative for PNP Transistors
- These are Pb−Free Devices*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector − Emitter Voltage 2N6515 2N6517, 2N6520	V_{CEO}	 250 350	Vdc
Collector − Base Voltage 2N6515 2N6517, 2N6520	V_{CBO}	 250 350	Vdc
Emitter − Base Voltage 2N6515, 2N6517 2N6520	V_{EBO}	 6.0 5.0	Vdc
Base Current	I_B	250	mAdc
Collector Current − Continuous	I_C	500	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	83.3	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
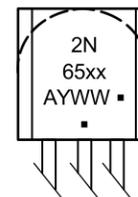
COLLECTOR 3
2 BASE
NPN
1 EMITTER

COLLECTOR 3
2 BASE
PNP
1 EMITTER

**TO−92
CASE 29
STYLE 1**

STRAIGHT LEAD
BULK PACK

BENT LEAD
TAPE & REEL
AMMO PACK

MARKING DIAGRAM

2N
65xx
AYWW ▪
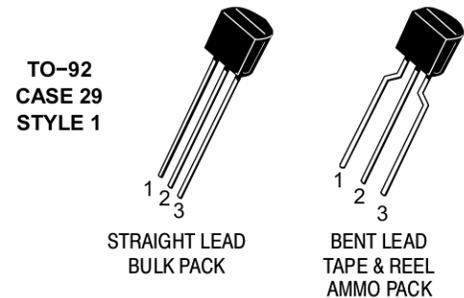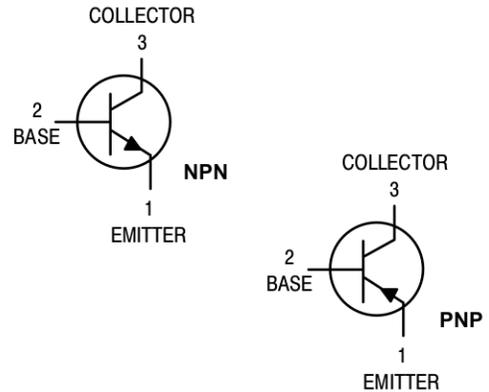
xx = 15, 17, or 20
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

NPN − 2N6515, 2N6517; PNP − 2N6520

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Breakdown Voltage (Note 1) (I_C = 1.0 mAdc, I_B = 0) 2N6515 2N6517, 2N6520	$V_{(BR)CEO}$	250 350	− −	Vdc
Collector−Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0) 2N6515 2N6517, 2N6520	$V_{(BR)CBO}$	250 350	− −	Vdc
Emitter−Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0) 2N6515, 2N6517 2N6520	$V_{(BR)EBO}$	6.0 5.0	− −	Vdc
Collector Cutoff Current (V_{CB} = 150 Vdc, I_E = 0) 2N6515 (V_{CB} = 250 Vdc, I_E = 0) 2N6517, 2N6520	I_{CBO}	− −	50 50	nAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0) 2N6515, 2N6517 (V_{EB} = 4.0 Vdc, I_C = 0) 2N6520	I_{EBO}	− −	50 50	nAdc
ON CHARACTERISTICS (Note 1)				
DC Current Gain (I_C = 1.0 mAdc, V_{CE} = 10 Vdc) 2N6515 2N6517, 2N6520	h_{FE}	35 20	− −	−
(I_C = 10 mAdc, V_{CE} = 10 Vdc) 2N6515 2N6517, 2N6520		50 30	− −	
(I_C = 30 mAdc, V_{CE} = 10 Vdc) 2N6515 2N6517, 2N6520		50 30	300 200	
(I_C = 50 mAdc, V_{CE} = 10 Vdc) 2N6515 2N6517, 2N6520		45 20	220 200	
(I_C = 100 mAdc, V_{CE} = 10 Vdc) 2N6515 2N6517, 2N6520		25 15	− −	
Collector−Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc) (I_C = 20 mAdc, I_B = 2.0 mAdc) (I_C = 30 mAdc, I_B = 3.0 mAdc) (I_C = 50 mAdc, I_B = 5.0 mAdc)	$V_{CE(sat)}$	− − − −	0.30 0.35 0.50 1.0	Vdc
Base−Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc) (I_C = 20 mAdc, I_B = 2.0 mAdc) (I_C = 30 mAdc, I_B = 3.0 mAdc)	$V_{BE(sat)}$	− − −	0.75 0.85 0.90	Vdc
Base−Emitter On Voltage (I_C = 100 mAdc, V_{CE} = 10 Vdc)	$V_{BE(on)}$	−	2.0	Vdc
SMALL−SIGNAL CHARACTERISTICS				
Current−Gain − Bandwidth Product (Note 1) (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 20 MHz)	f_T	40	200	MHz
Collector−Base Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	−	6.0	pF
Emitter−Base Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz) 2N6515, 2N6517 2N6520	C_{eb}	− −	80 100	pF
SWITCHING CHARACTERISTICS				
Turn−On Time (V_{CC} = 100 Vdc, $V_{BE(off)}$ = 2.0 Vdc, I_C = 50 mAdc, I_{B1} = 10 mAdc)	t_{on}	−	200	μs
Turn−Off Time (V_{CC} = 100 Vdc, I_C = 50 mAdc, I_{B1} = I_{B2} = 10 mAdc)	t_{off}	−	3.5	μs

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
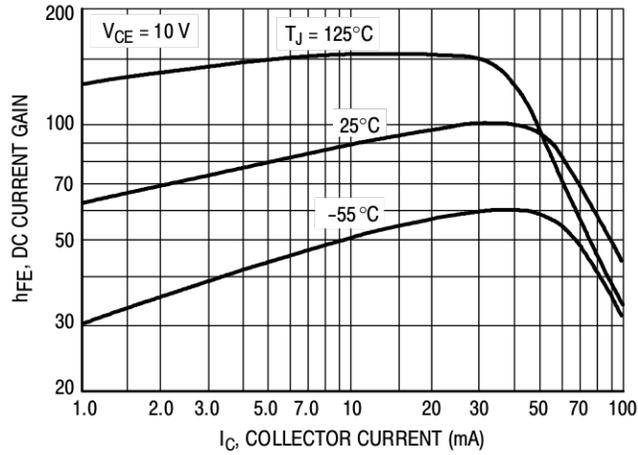
NPN − 2N6515, 2N6517; PNP − 2N6520
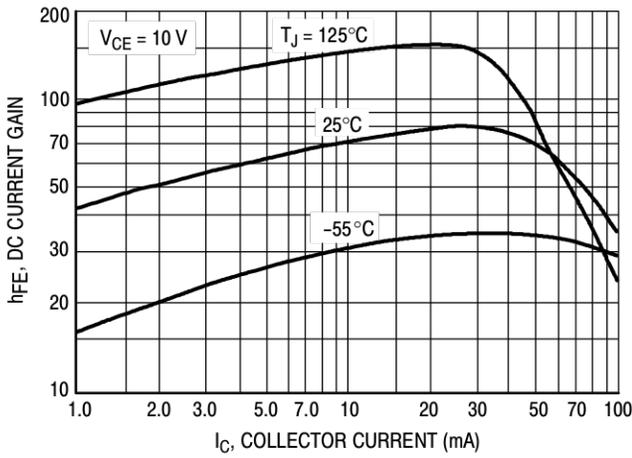
Figure 1. DC Current Gain
NPN 2N6515
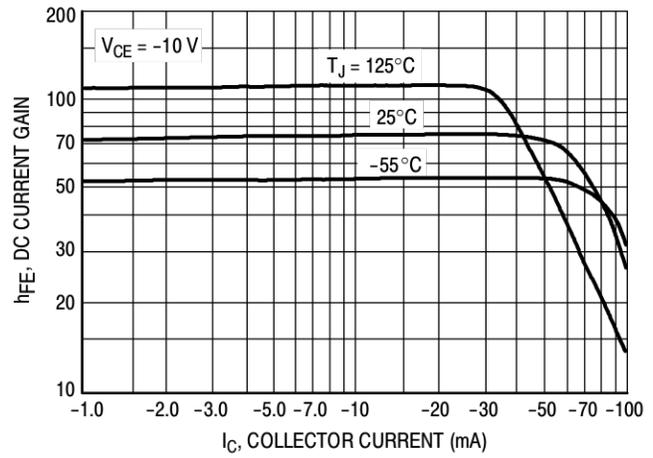
Figure 2. DC Current Gain
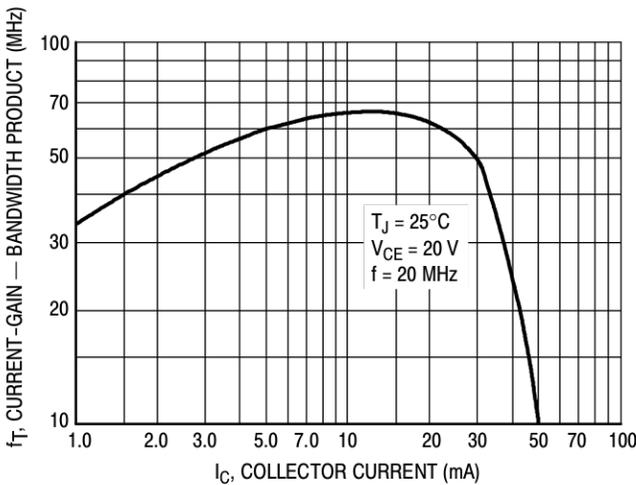**NPN 2N6517**

Figure 3. DC Current Gain
PNP 2N6520
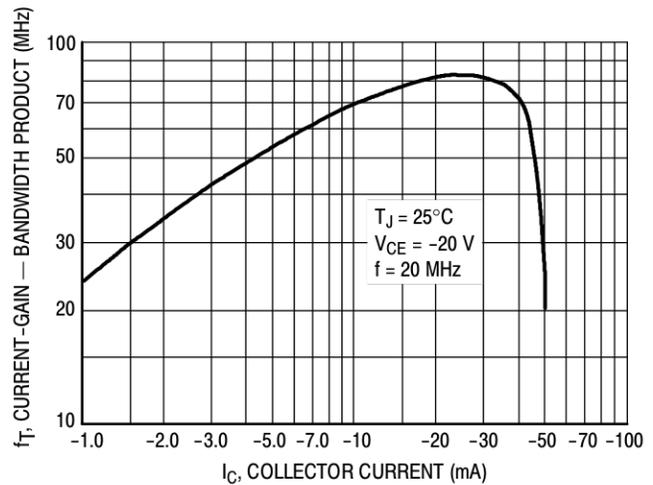
Figure 4. Current−Gain − Bandwidth Product
NPN 2N6515, 2N6517

Figure 5. Current−Gain − Bandwidth Product
PNP 2N6520

$T_J = 25°C$

$V_{BE(sat)}$ @ $I_C/I_B = 10$

$V_{BE(on)}$ @ $V_{CE} = 10$ V

$V_{CE(sat)}$ @ $I_C/I_B = 10$

$V_{CE(sat)}$ @ $I_C/I_B = 5.0$

V, VOLTAGE (VOLTS)

I_C, COLLECTOR CURRENT (mA)

Figure 6. "On" Voltages
NPN 2N6515, 2N6517

$T_J = 25°C$

$V_{BE(sat)}$ @ $I_C/I_B = 10$

$V_{BE(on)}$ @ $V_{CE} = -10$ V

$V_{CE(sat)}$ @ $I_C/I_B = 10$

$V_{CE(sat)}$ @ $I_C/I_B = 5.0$

V, VOLTAGE (VOLTS)

I_C, COLLECTOR CURRENT (mA)
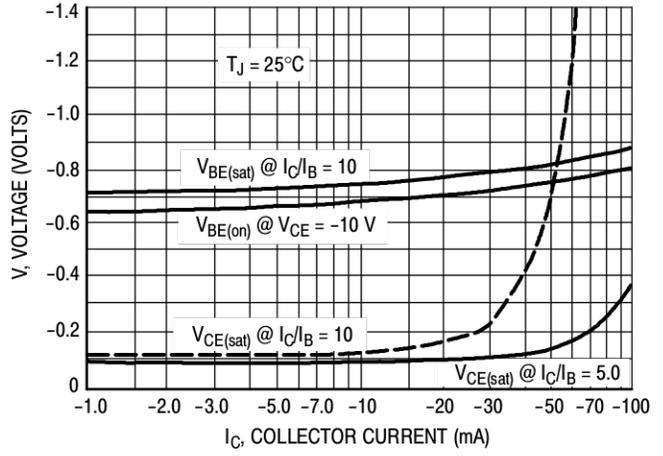
Figure 7. "On" Voltages
PNP 2N6520

$\dfrac{I_C}{I_B} = 10$

$R_{\theta VC}$ for $V_{CE(sat)}$

25°C to 125°C

−55°C to 25°C

−55°C to 125°C

$R_{\theta VB}$ for V_{BE}

$R_{\theta V}$, TEMPERATURE COEFFICIENTS (mV/°C)

I_C, COLLECTOR CURRENT (mA)
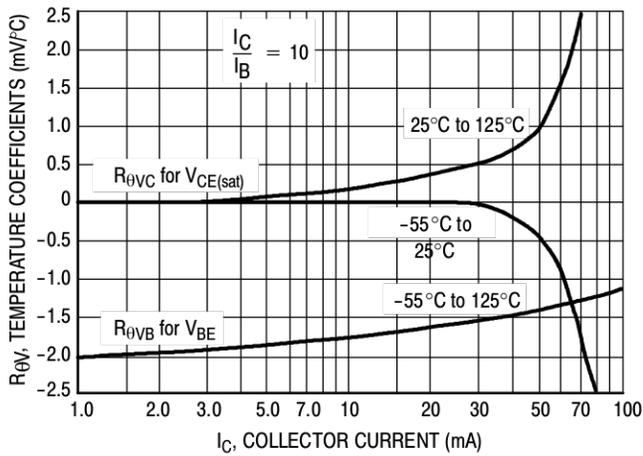
Figure 8. Temperature Coefficients
NPN 2N6515, 2N6517

$\dfrac{I_C}{I_B} = 10$

$R_{\theta VB}$ for V_{BE}

25°C to 125°C

−55°C to 25°C

$R_{\theta VC}$ for $V_{CE(sat)}$

−55°C to 125°C

$R_{\theta V}$, TEMPERATURE COEFFICIENTS (mV/°C)

I_C, COLLECTOR CURRENT (mA)
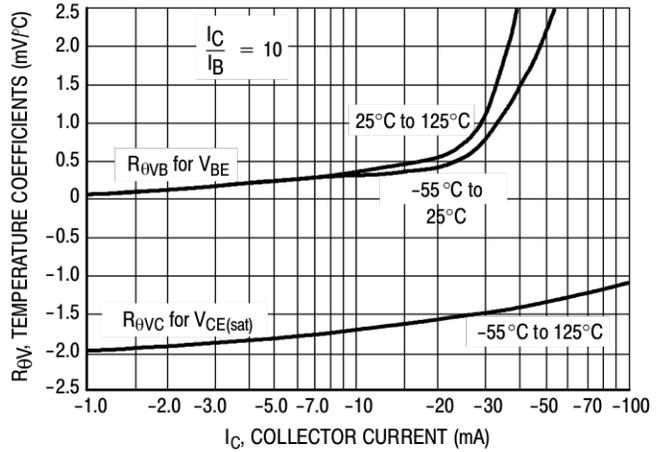
Figure 9. Temperature Coefficients
PNP 2N6520

$T_J = 25°C$

C_{eb}

C_{cb}

C, CAPACITANCE (pF)

V_R, REVERSE VOLTAGE (VOLTS)
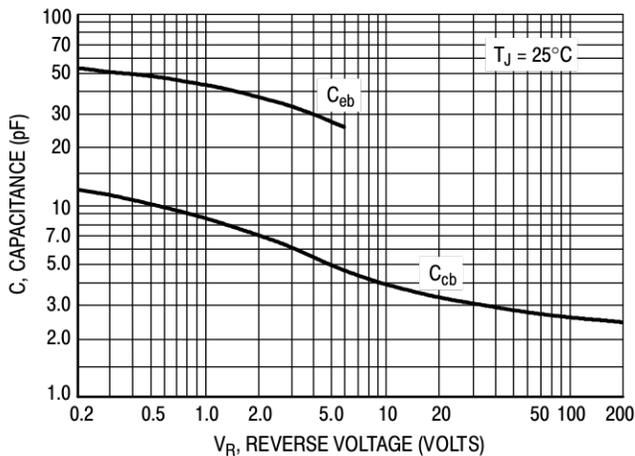
Figure 10. Capacitance
NPN 2N6515, 2N6517

C_{eb}

$T_J = 25°C$

C_{cb}

C, CAPACITANCE (pF)
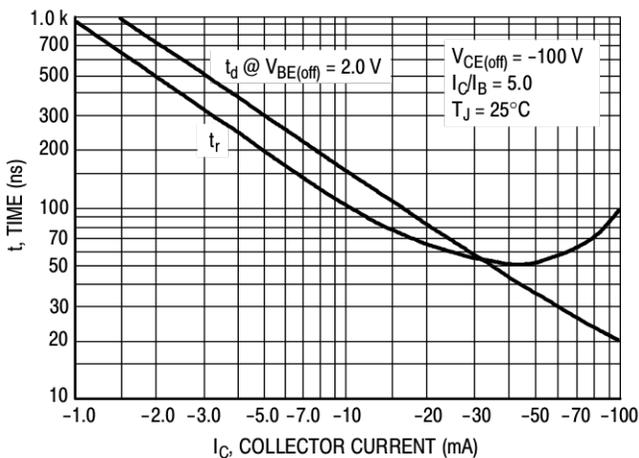
V_R, REVERSE VOLTAGE (VOLTS)
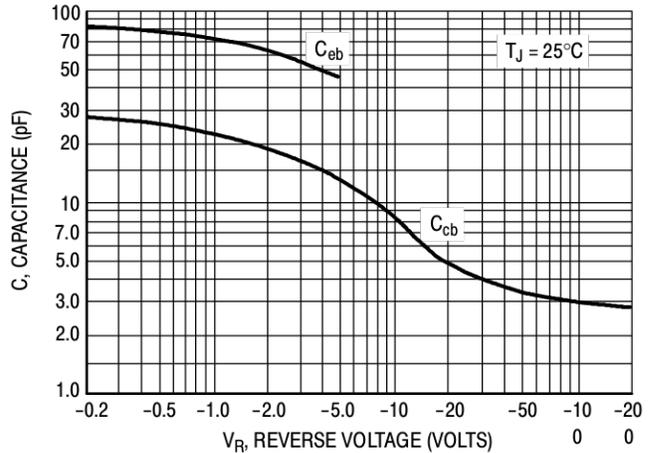
Figure 11. Capacitance
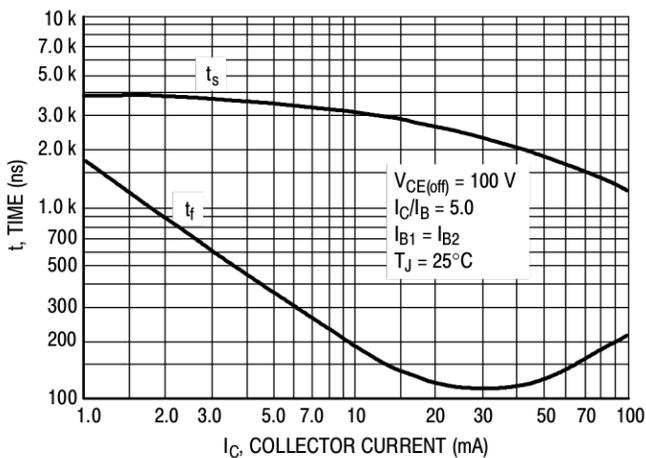**PNP 2N6520**

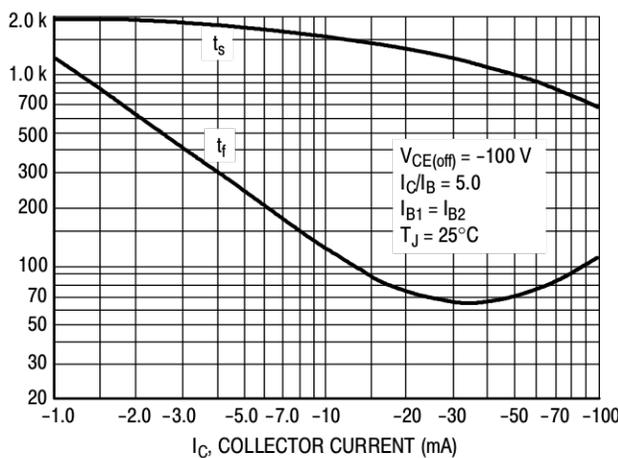# NPN − 2N6515, 2N6517; PNP − 2N6520
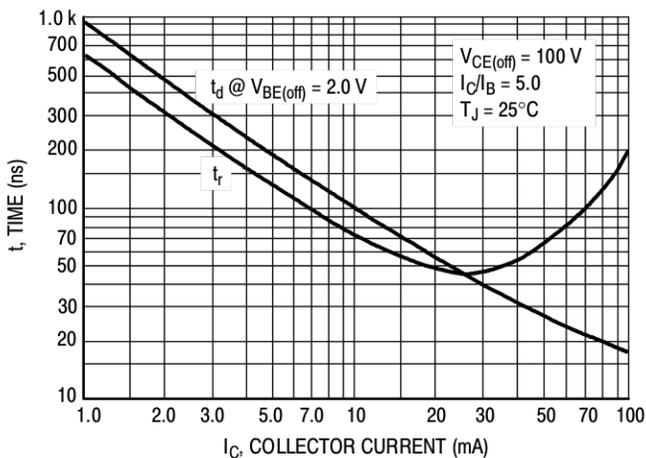
Figure 12. Turn−On Time
NPN 2N6515, 2N6517

Figure 13. Turn−On Time
PNP 2N6520

Figure 14. Turn−Off Time
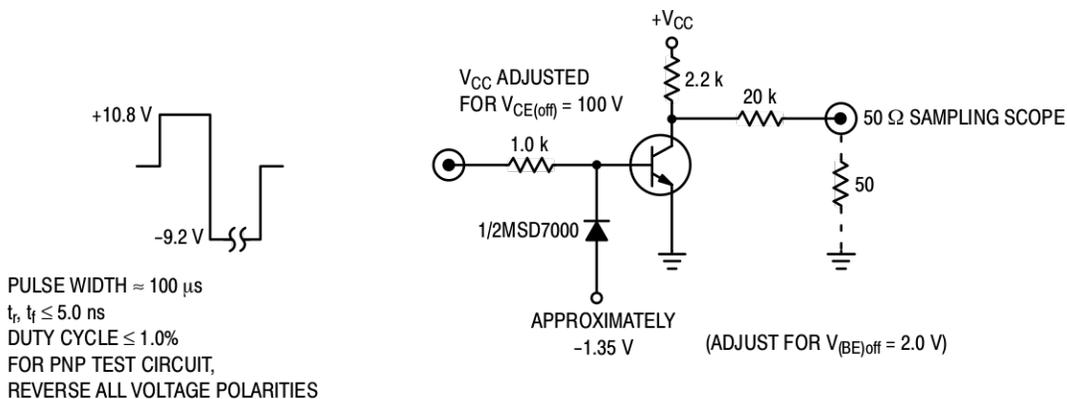**NPN 2N6515, 2N6517**

Figure 15. Turn−Off Time
PNP 2N6520

+10.8 V

−9.2 V

PULSE WIDTH ≈ 100 μs
t_r, t_f ≤ 5.0 ns
DUTY CYCLE ≤ 1.0%
FOR PNP TEST CIRCUIT,
REVERSE ALL VOLTAGE POLARITIES

$+V_{CC}$

V_{CC} ADJUSTED
FOR $V_{CE(off)}$ = 100 V

2.2 k

20 k

50 Ω SAMPLING SCOPE

1.0 k

50

1/2MSD7000

APPROXIMATELY
−1.35 V

(ADJUST FOR $V_{(BE)off}$ = 2.0 V)

Figure 16. Switching Time Test Circuit
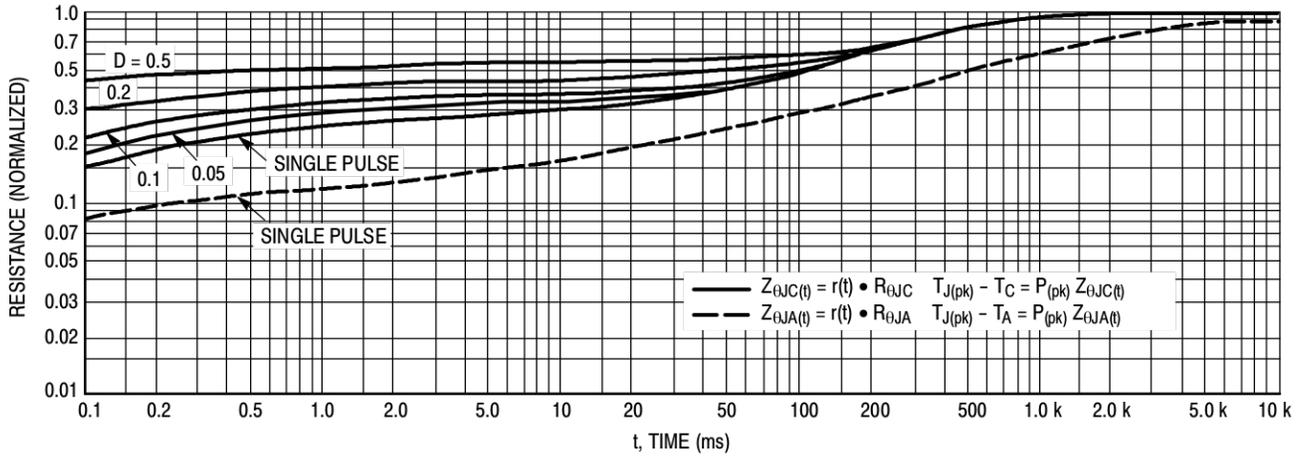
Figure 17. Thermal Response
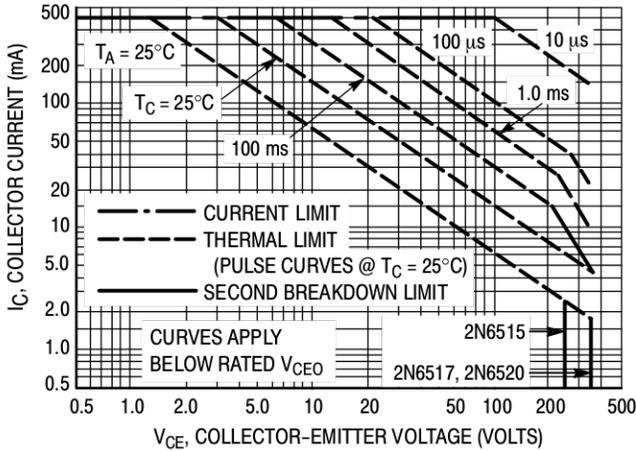
Figure 18. Active Region Safe Operating Area

FIGURE A

$$\text{DUTY CYCLE} = t_1 \, f = \frac{t_1}{t_P}$$

PEAK PULSE POWER = P_P
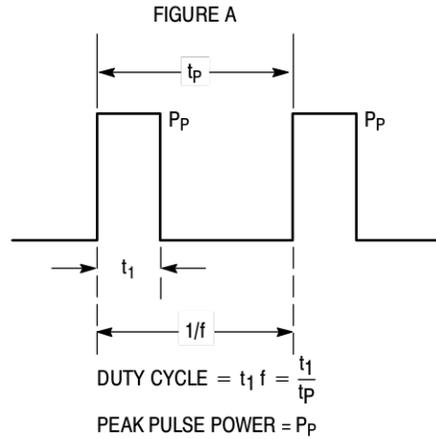
Design Note: Use of Transient Thermal Resistance Data

ORDERING INFORMATION

Device	Package	Shipping[†]
2N6515RLRMG	TO−92 (Pb−Free)	2000 Ammo Pack
2N6517G	TO−92 (Pb−Free)	5000 Unit / Bulk
2N6517RLRPG	TO−92 (Pb−Free)	2000 Ammo Pack
2N6520RLRAG	TO−92 (Pb−Free)	2000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SCALE 1:1

1 2 3
STRAIGHT LEAD
BULK PACK

1 2 3
BENT LEAD
TAPE & REEL
AMMO PACK
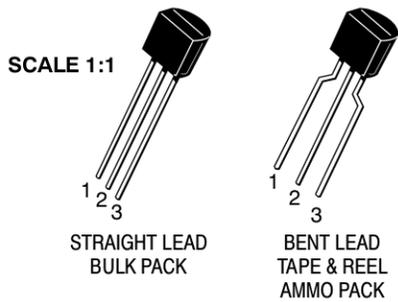
TO−92 (TO−226)
CASE 29−11
ISSUE AM

DATE 09 MAR 2007

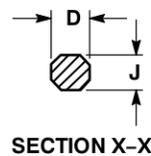STRAIGHT LEAD
BULK PACK

SEATING
PLANE

SECTION X−X
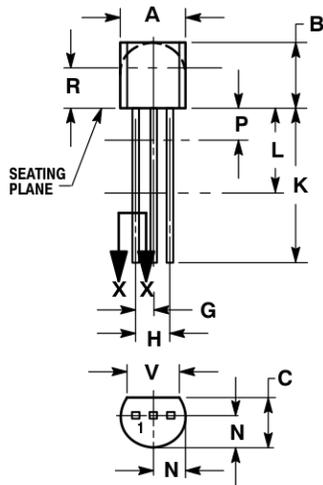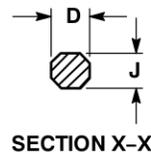
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---

BENT LEAD
TAPE & REEL
AMMO PACK

SEATING
PLANE

SECTION X−X
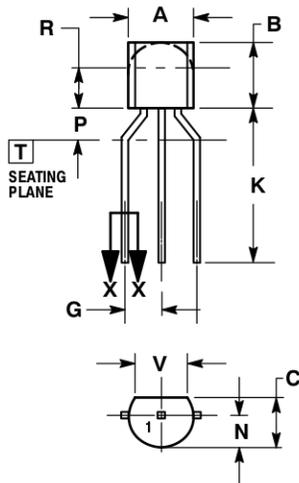
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	4.45	5.20
B	4.32	5.33
C	3.18	4.19
D	0.40	0.54
G	2.40	2.80
J	0.39	0.50
K	12.70	---
N	2.04	2.66
P	1.50	4.00
R	2.93	---
V	3.43	---

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42022B	
STATUS:	**ON SEMICONDUCTOR STANDARD**	
NEW STANDARD:		
DESCRIPTION:	TO−92 (TO−226)	PAGE 1 OF 3

STYLE 1:
PIN 1. EMITTER
   2. BASE
   3. COLLECTOR

STYLE 2:
PIN 1. BASE
   2. EMITTER
   3. COLLECTOR

STYLE 3:
PIN 1. ANODE
   2. ANODE
   3. CATHODE

STYLE 4:
PIN 1. CATHODE
   2. CATHODE
   3. ANODE

STYLE 5:
PIN 1. DRAIN
   2. SOURCE
   3. GATE

STYLE 6:
PIN 1. GATE
   2. SOURCE & SUBSTRATE
   3. DRAIN

STYLE 7:
PIN 1. SOURCE
   2. DRAIN
   3. GATE

STYLE 8:
PIN 1. DRAIN
   2. GATE
   3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
   2. EMITTER
   3. BASE 2

STYLE 10:
PIN 1. CATHODE
   2. GATE
   3. ANODE

STYLE 11:
PIN 1. ANODE
   2. CATHODE & ANODE
   3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
   2. GATE
   3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
   2. GATE
   3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
   2. COLLECTOR
   3. BASE

STYLE 15:
PIN 1. ANODE 1
   2. CATHODE
   3. ANODE 2

STYLE 16:
PIN 1. ANODE
   2. GATE
   3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
   2. BASE
   3. EMITTER

STYLE 18:
PIN 1. ANODE
   2. CATHODE
   3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
   2. ANODE
   3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
   2. CATHODE
   3. ANODE

STYLE 21:
PIN 1. COLLECTOR
   2. EMITTER
   3. BASE

STYLE 22:
PIN 1. SOURCE
   2. GATE
   3. DRAIN

STYLE 23:
PIN 1. GATE
   2. SOURCE
   3. DRAIN

STYLE 24:
PIN 1. EMITTER
   2. COLLECTOR/ANODE
   3. CATHODE

STYLE 25:
PIN 1. MT 1
   2. GATE
   3. MT 2

STYLE 26:
PIN 1. V_{CC}
   2. GROUND 2
   3. OUTPUT

STYLE 27:
PIN 1. MT
   2. SUBSTRATE
   3. MT

STYLE 28:
PIN 1. CATHODE
   2. ANODE
   3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
   2. ANODE
   3. CATHODE

STYLE 30:
PIN 1. DRAIN
   2. GATE
   3. SOURCE

STYLE 31:
PIN 1. GATE
   2. DRAIN
   3. SOURCE

STYLE 32:
PIN 1. BASE
   2. COLLECTOR
   3. EMITTER

STYLE 33:
PIN 1. RETURN
   2. INPUT
   3. OUTPUT

STYLE 34:
PIN 1. INPUT
   2. GROUND
   3. LOGIC

STYLE 35:
PIN 1. GATE
   2. COLLECTOR
   3. EMITTER

DOCUMENT NUMBER:	98ASB42022B	
STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	TO−92 (TO−226)	PAGE 2 OF 3

ISSUE	REVISION	DATE
AM	ADDED BENT–LEAD TAPE & REEL VERSION. REQ. BY J. SUPINA.	09 MAR 2007

PUBLICATION ORDERING INFORMATION

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