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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD SEMICONDUCTOR®

February 2008

74LVX74
Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop

Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance

General Description

The LVX74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:

- LOW input to $\overline{S}_D$ (Set) sets Q to HIGH level
- LOW input to $\overline{C}_D$ (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

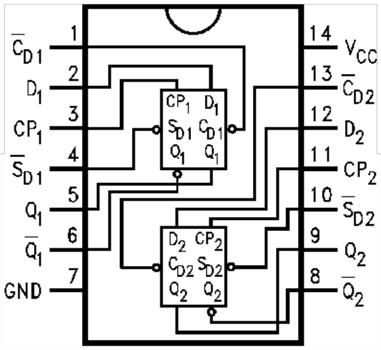
Ordering Information

Order Number	Package Number	Package Description
74LVX74M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LVX74SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVX74MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

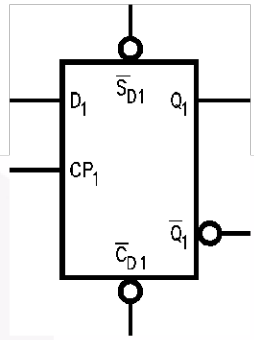
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

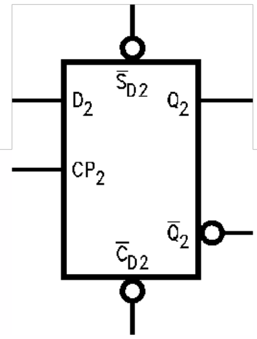
All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram

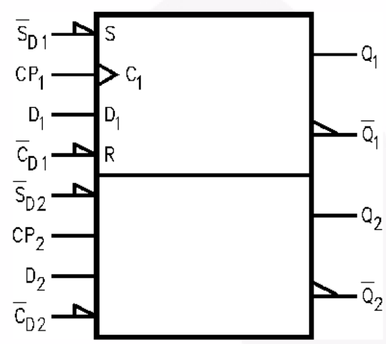


Logic Symbols





IEEE/IEC



Pin Description

Pin Names	Description
D_1, D_2	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs

Truth Table

(Each Half)

Inputs				Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	$\nearrow$	H	H	L
H	H	$\nearrow$	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

$\nearrow$ = LOW-to-HIGH Clock Transition

$Q_0(\overline{Q}_0)$ = Previous $Q(\overline{Q})$ before LOW-to-HIGH Transition of Clock

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
I_{IK}	DC Input Diode Current, $V_I = –0.5V$	–20mA
V_I	DC Input Voltage	–0.5V to 7V
I_{OK}	DC Output Diode Current	
	$V_O = –0.5V$	–20mA
	$V_O = V_{CC} + 0.5V$	+20mA
V_O	DC Output Voltage	–0.5V to V_{CC} + 0.5V
I_O	DC Output Source or Sink Current	±25mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	±50mA
T_{STG}	Storage Temperature	–65°C to +150°C
P	Power Dissipation	180mW

Recommended Operating Conditions(1)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	2.0V to 3.6V
V_I	Input Voltage	0V to 5.5V
V_O	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	–40°C to +85°C
$\Delta t / \Delta V$	Input Rise and Fall Time	0ns/V to 100ns/V

Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	Conditions	$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		Units
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	HIGH Level Input Voltage	2.0		1.5			1.5		V
		3.0		2.0			2.0		
		3.6		2.4			2.4		
V_{IL}	LOW Level Input Voltage	2.0				0.5		0.5	V
		3.0				0.8		0.8	
		3.6				0.8		0.8	
V_{OH}	HIGH Level Output Voltage	2.0	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OH} = -50\mu A$	1.9	2.0		1.9		V
		3.0	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OH} = -50\mu A$	2.9	3.0		2.9		
			$V_{IN} = V_{IL}$ or V_{IH}, $I_{OH} = -4mA$	2.58			2.48		
V_{OL}	LOW Level Output Voltage	2.0	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OL} = 50\mu A$		0.0	0.1		0.1	V
		3.0	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OL} = 50\mu A$		0.0	0.1		0.1	
			$V_{IN} = V_{IL}$ or V_{IH}, $I_{OL} = 4mA$			0.36		0.44	
I_{IN}	Input Leakage Current	3.6	$V_{IN} = 5.5V$ or GND			±0.1		±1.0	µA
I_{CC}	Quiescent Supply Current	3.6	$V_{IN} = V_{CC}$ or GND			2.0		20.0	µA

Noise Characteristics(2)

Symbol	Parameter	V_{CC} (V)	C_L (pF)	$T_A = 25°C$		Units
				Typ.	Limit	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	50	0.3	0.5	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	50	–0.3	–0.5	V
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	3.3	50		2.0	V
V_{ILD}	Maximum LOW Level Dynamic Input Voltage	3.3	50		0.8	V

Note:

2. Input $t_r = t_f = 3ns$

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	C_L (pF)	$T_A = +25°C$			$T_A = –40°C$ to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay, CP_n to Q_n or $\overline{Q}_n$	2.7	15		7.3	15	1.0	18.5	ns
			50		9.8	18.5	1.0	22	
		3.3 ± 0.3	15		5.7	9.7	1.0	11.5	
			50		8.2	13.2	1.0	15	
t_{PLH}, t_{PHL}	Propagation Delay, $\overline{C}_{Dn}$ to $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	2.7	15		8.4	15.6	1.0	18.5	ns
			50		10.9	19.1	1.0	22	
		3.3 ± 0.3	15		6.6	10.1	1.0	12	
			50		9.1	13.6	1.0	15.5	
t_W	CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width	2.7		8.5			10		ns
		3.3 ± 0.3		6			7		
t_S	Setup Time, D_n to CP_n	2.7		8.0			9.5		ns
		3.3 ± 0.3		5.5			6.5		
t_H	Hold Time, D_n to CP_n	2.7		0.5			0.5		ns
		3.3 ± 0.3		0.5			0.5		
t_{REC}	Recovery Time, $\overline{CP}_n$ or $\overline{S}_{Dn}$ to CP_n	2.7		6.5			7.5		ns
		3.3 ± 0.3		5.0			5.0		
f_{MAX}	Maximum Clock Frequency	2.7	15	55	135		50		MHz
			50	45	60		40		
		3.3 ± 0.3	15	95	145		80		
			50	60	85		50		
t_{OSLH}, t_{OSHL}	Output to Output Skew(3)	2.7	50			1.5		1.5	ns
		3.3				1.5		1.5	

Note:

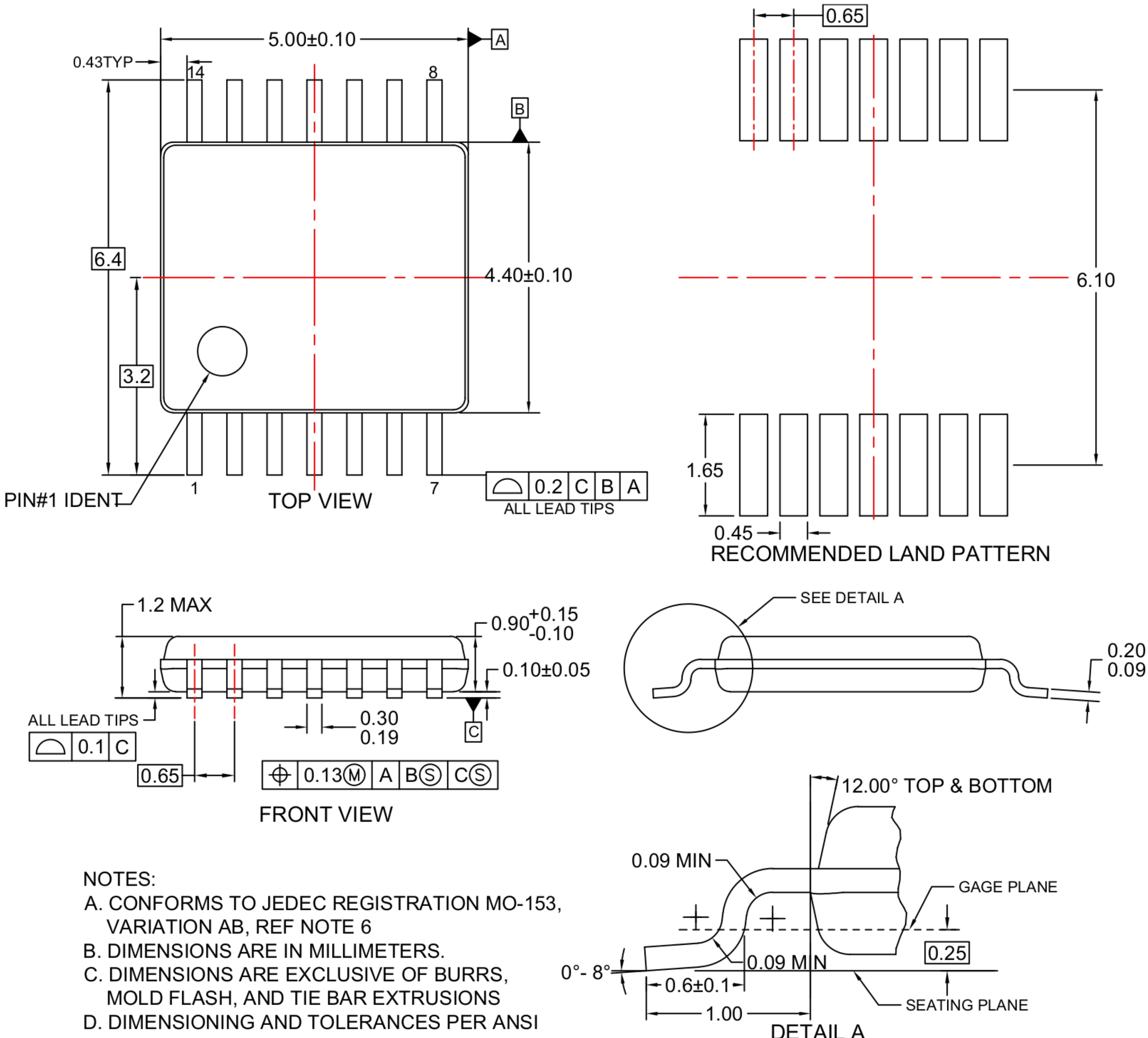
3. Parameter guaranteed by design $t_{OSLH} = |t_{PLHm} – t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} – t_{PHLn}|$

Capacitance

Symbol	Parameter	$T_A = +25°C$			$T_A = –40°C$ to +85°C		Units
		Min.	Typ.	Max.	Min.	Max.	
C_{IN}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance(4)		25				pF

Note:

4. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the eqation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} \times I_{CC}}{2 (per\_F/F)}$



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 2009.
E. LANDPATTERN STANDARD: SOP65P640X110-14M.
F. DRAWING FILE NAME: MKT-MTC14rev7.

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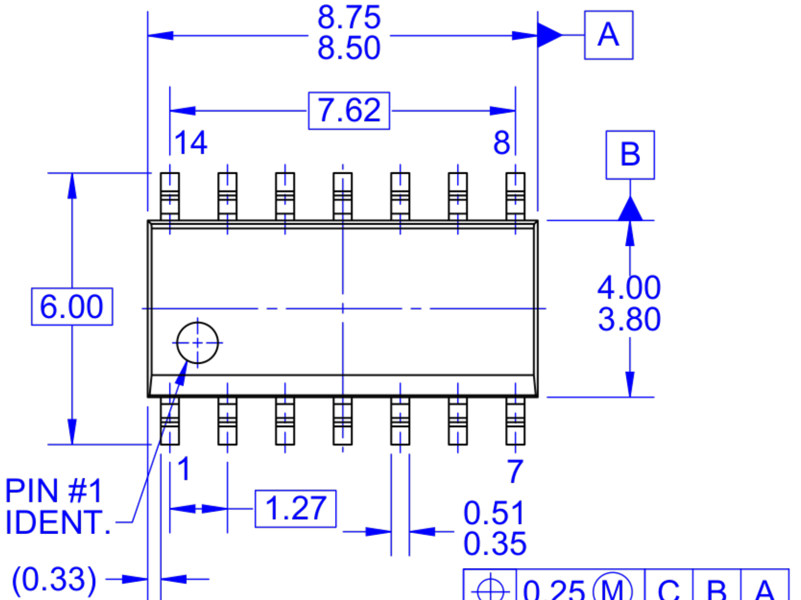
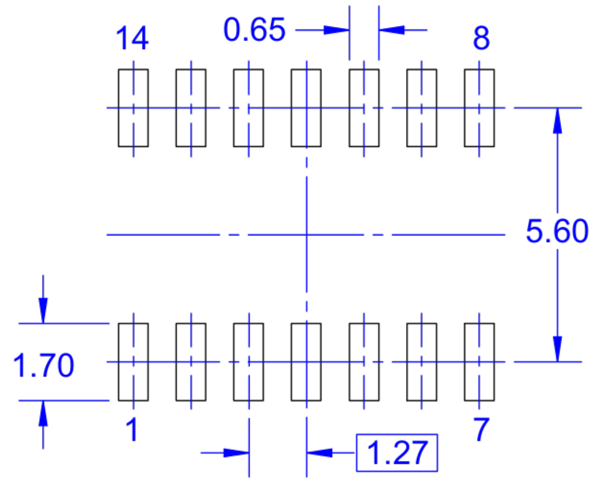
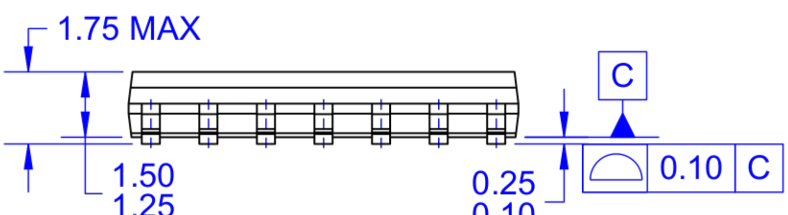


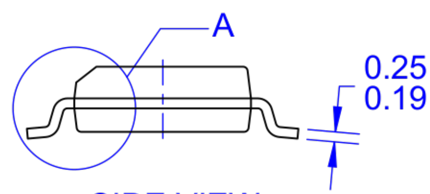
TOP VIEW



LAND PATTERN RECOMMENDATION



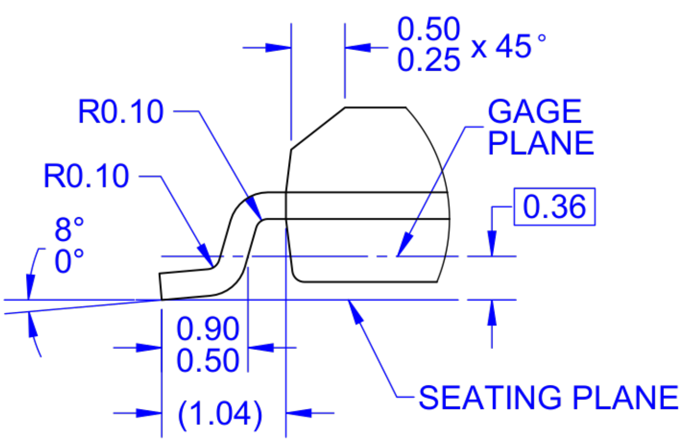
FRONT VIEW



SIDE VIEW

NOTES:

A. CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
D. LAND PATTERN STANDARD: SOIC127P600X145-14M
E. CONFORMS TO ASME Y14.5M, 2009
D. DRAWING FILENAME: MKT-M14Arev14



DETAIL A
SCALE 16 : 1

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