Is Now Part of

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD SEMICONDUCTOR™

October 1995
Revised August 2004

NC7S02
TinyLogic™ HS 2-Input NOR Gate

General Description

The NC7S02 is a single 2-Input high performance CMOS NOR Gate. Advanced Silicon Gate CMOS fabrication assures high speed and low power circuit operation over a broad V_{CC} range. ESD protection diodes inherently guard both inputs and output with respect to the V_{CC} and GND rails. Three stages of gain between inputs and outputs assures high noise immunity and reduced sensitivity to input edge rate.

Features

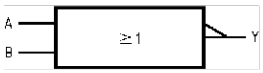
- Space saving SOT23 or SC70 5-lead packages
- Ultra small MicroPak™ leadless package
- High Speed; t_{PD} 3.5 ns typ
- Low Quiescent Power; I_{CC} <1 µA
- Balanced Output Drive; 2 mA I_{OL}, –2 mA I_{OH}
- Broad V_{CC} Operating Range; 2V–6V
- Balanced Propagation Delays
- Specified for 3V operation

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7S02M5X	MA05B	7S02	5-Lead SOT23, JEDEC MO-178, 1.6mm	3k Units on Tape and Reel
NC7S02P5X	MAA05A	S02	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3k Units on Tape and Reel
NC7S02L6X	MAC06A	E4	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel

Logic Symbol

IEEE/IEC



Pin Descriptions

Pin Names	Description
A, B	Inputs
Y	Output
NC	No Connect

Function Table

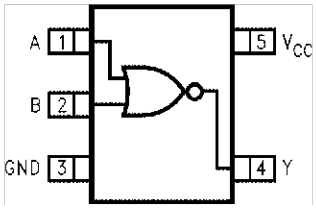
$Y = \overline{A + B}$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H =HIGH Logic Level
L =LOW Logic Level

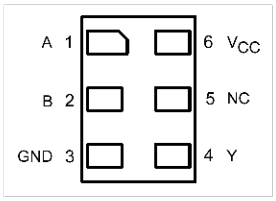
Connection Diagrams

Pin Assignments for SOT23 and SC70



(Top View)

Pad Assignments for MicroPak



(Top Through View)

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
@ $V_{IN} \leq -0.5V$	−20 mA
@ $V_{IN} \geq V_{CC}$ +0.5V	+20 mA
DC Input Voltage (V_{IN})	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_{OK})	
@ $V_{OUT} < -0.5V$	−20 mA
@ $V_{OUT} > V_{CC}$ +0.5V	+20 mA
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} +0.5V
DC Output Source	
or Sink Current (I_{OUT})	±12.5 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±25 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	150°C
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C
Power Dissipation (P_D) @ +85°C	
SOT23-5	200 mW
SC70-5	150 mW

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{CC})	2.0V to 6.0V
Input Voltage (V_{IN})	0V to V_{CC}
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} @ 2.0V	0 to 1000 ns
V_{CC} @ 3.0V	0 to 750 ns
V_{CC} @ 4.5V	0 to 500 ns
V_{CC} @ 6.0V	0 to 400 ns
Thermal Resistance (θ_{JA})	
SOT23-5	300°C/W
SC70-5	425°C/W

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of circuits outside databook specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

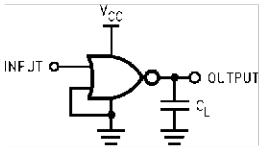
Symbol	Parameter	V_{CC}	T_A = +25°C			T_A = −40°C to +85°C		Units	Conditions
		(V)	Min	Typ	Max	Min	Max		
V_{IH}	HIGH Level Input Voltage	2.0	1.50			1.50		V	
		3.0-6.0	0.7 V_{CC}			0.7 V_{CC}			
V_{IL}	LOW Level Input Voltage	2.0			0.50		0.50	V	
		3.0-6.0			0.3 V_{CC}		0.3 V_{CC}		
V_{OH}	HIGH Level Output Voltage	2.0	1.90	2.0		1.90		V	I_{OH} = −20 µA V_{IN} = V_{IL}
		3.0	2.90	3.0		2.90			
		4.5	4.40	4.5		4.40			
		6.0	5.90	6.0		5.90			
								V	V_{IN} = V_{IL}
		3.0	2.68	2.85		2.63			I_{OH} = −1.3 mA
		4.5	4.18	4.35		4.13			I_{OH} = −2 mA
		6.0	5.68	5.85		5.63			I_{OH} = −2.6 mA
V_{OL}	LOW Level Output Voltage	2.0		0.0	0.10		0.10	V	I_{OL} = 20 µA V_{IN} = V_{IH}
		3.0		0.0	0.10		0.10		
		4.5		0.0	0.10		0.10		
		6.0		0.0	0.10		0.10		
								V	V_{IN} = V_{IH}
		3.0		0.1	0.26		0.33		I_{OL} = 1.3 mA
		4.5		0.1	0.26		0.33		I_{OL} = 2 mA
		6.0		0.1	0.26		0.33		I_{OL} = 2.6 mA
I_{IN}	Input Leakage Current	6.0			±0.1		±1.0	µA	V_{IN} = V_{CC}, GND
I_{CC}	Quiescent Supply Current	6.0			1.0		10.0	µA	V_{IN} = V_{CC}, GND

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions	Figure Number
			Min	Typ	Max	Min	Max			
t_{PLH}, t_{PHL}	Propagation Delay	5.0		3.5	15			ns	$C_L = 15$ pF	Figures 1, 3
		2.0		19	100		125	ns	$C_L = 50$ pF	
		3.0		10.5	27		35			
		4.5		7.5	20		25			
		6.0		6.5	17		21			
t_{TLH}, t_{THL}	Output Transition Time	5.0		3	10			ns	$C_L = 15$ pF	Figures 1, 3
		2.0		25	125		155	ns	$C_L = 50$ pF	
		3.0		16	35		45			
		4.5		11	25		31			
		6.0		9	21		26			
C_{IN}	Input Capacitance	Open		2	10		10	pF		
C_{PD}	Power Dissipation Capacitance	5.0		6				pF	(Note 3)	Figure 2

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CC}\text{static})$.

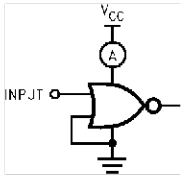
AC Loading and Waveforms



C_L includes load and stray capacitance

Input PRR = 1.0 MHz; t_w = 500 ns

FIGURE 1. AC Test Circuit



Input = AC Waveform;

PRR = variable; Duty Cycle = 50%

FIGURE 2. I_{CCD} Test Circuit

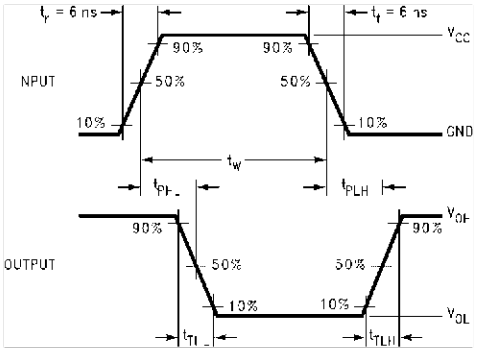


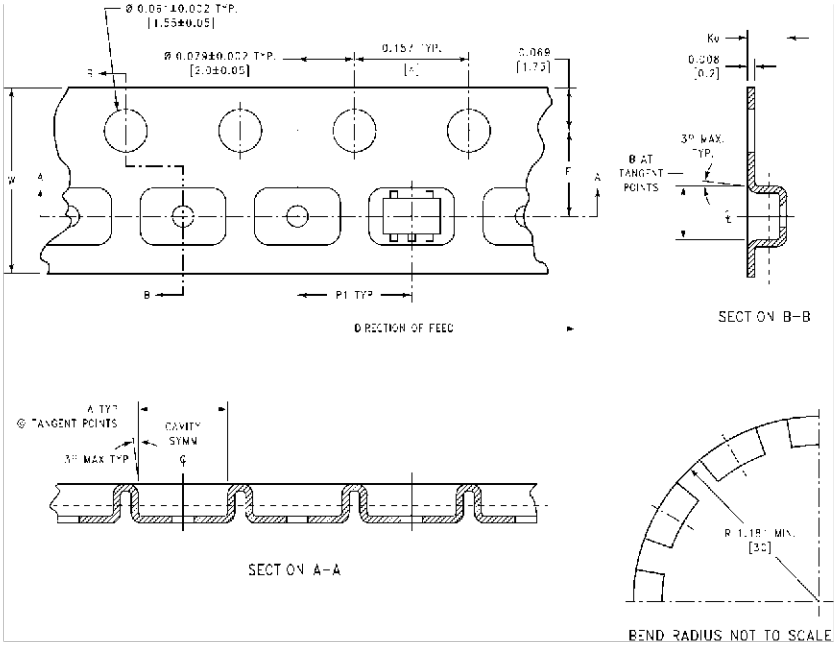
FIGURE 3. AC Waveforms

Tape and Reel Specification

TAPE FORMAT for SOT23 and SC70

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
M5X, P5X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)

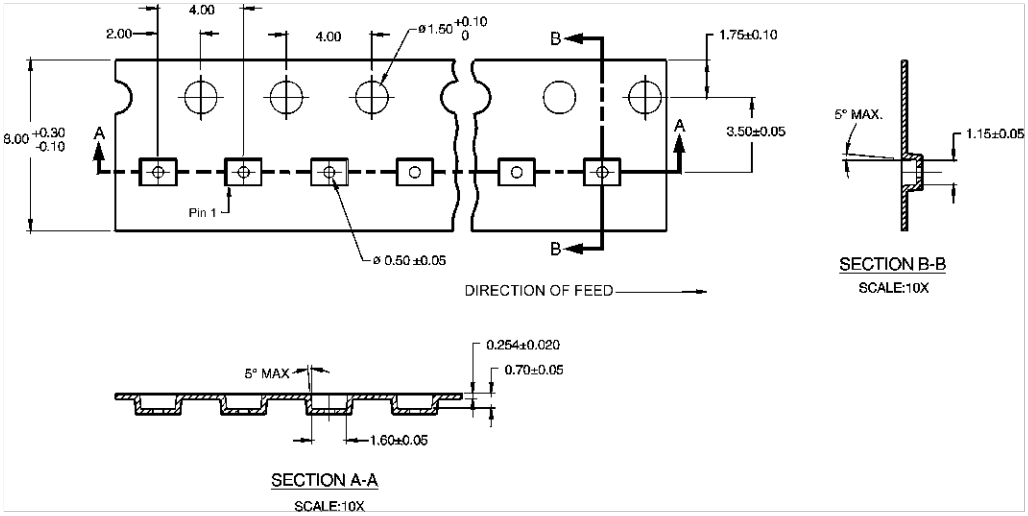


Package	Tape Size	DIM A	DIM B	DIM F	DIM K_o	DIM P1	DIM W
SC70-5	8 mm	0.093 (2.35)	0.096 (2.45)	0.138 ±0.004 (3.5 ±0.10)	0.053 ±0.004 (1.35 ±0.10)	0.157 (4)	0.315 ±0.004 (8 ±0.1)
SOT23-5	8 mm	0.130 (3.3)	0.130 (3.3)	0.138 ±0.002 (3.5 ±0.05)	0.055 ±0.004 (1.4 ±0.11)	0.157 (4)	0.315 ±0.012 (8 ±0.3)

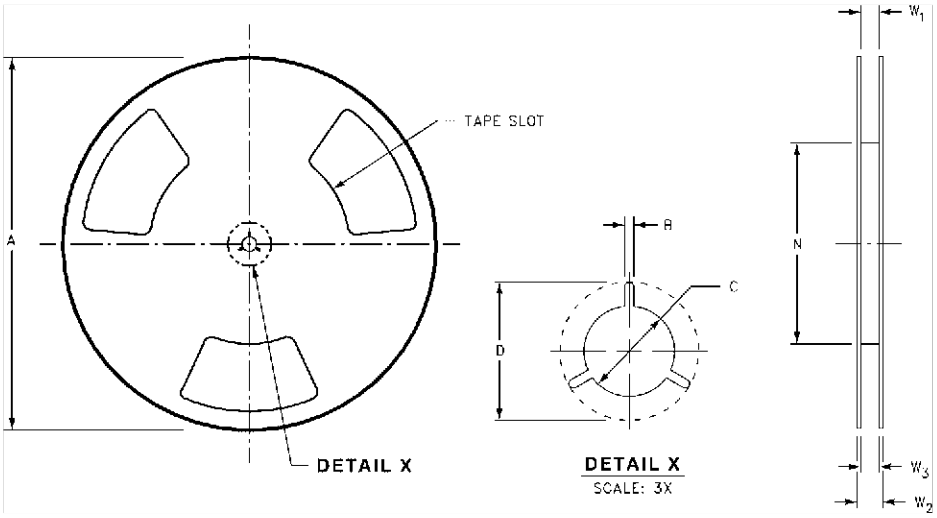
Tape and Reel Specification (Continued)

TAPE FORMAT for MicroPak

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L6X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

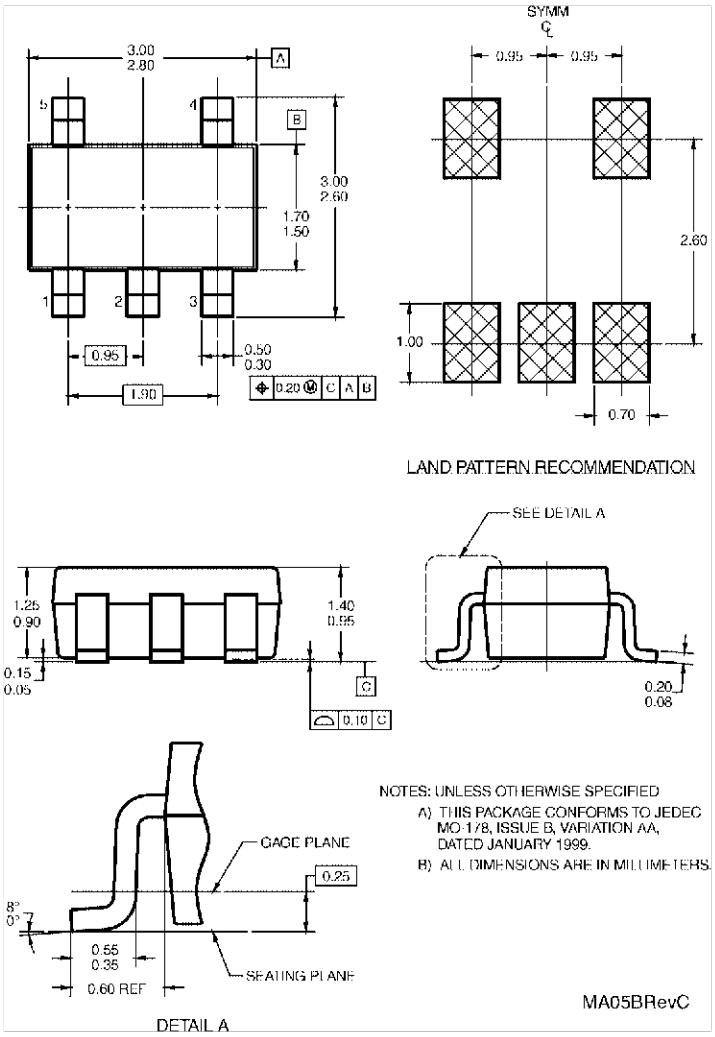


REEL DIMENSIONS inches (millimeters)



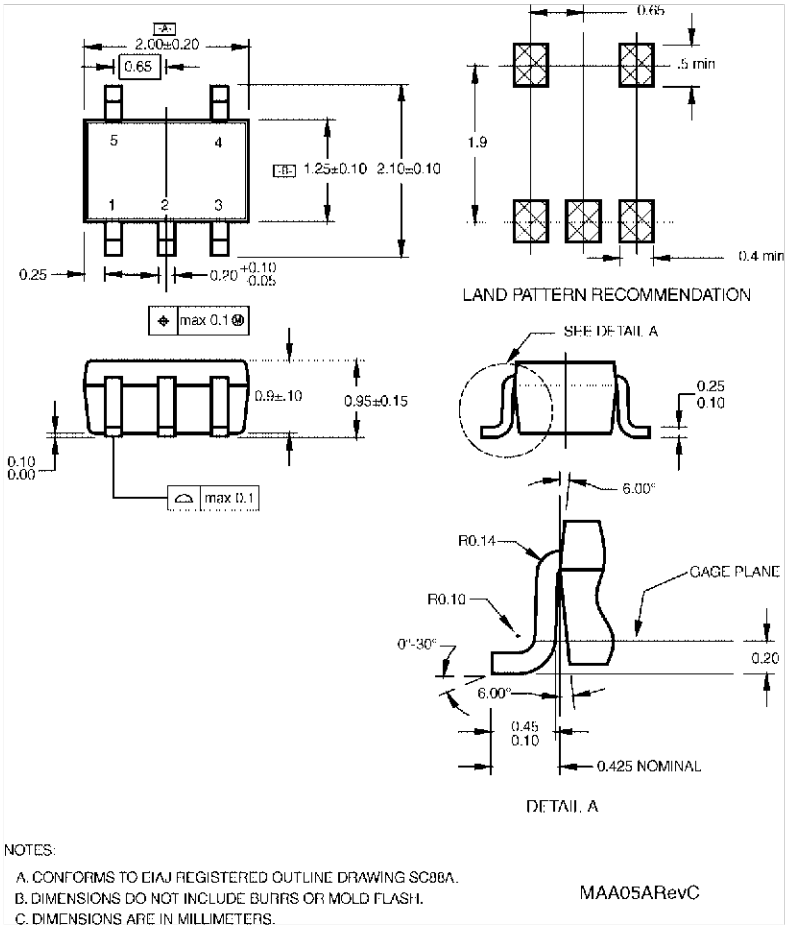
Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 +0.059/–0.000 (8.40 +1.50/–0.00)	0.567 (14.40)	W1 +0.078/–0.039 (W1 +2.00/–1.00)

Physical Dimensions inches (millimeters) unless otherwise noted



5-Lead SOT23, JEDEC MO-178, 1.6mm
Package Number MA05B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



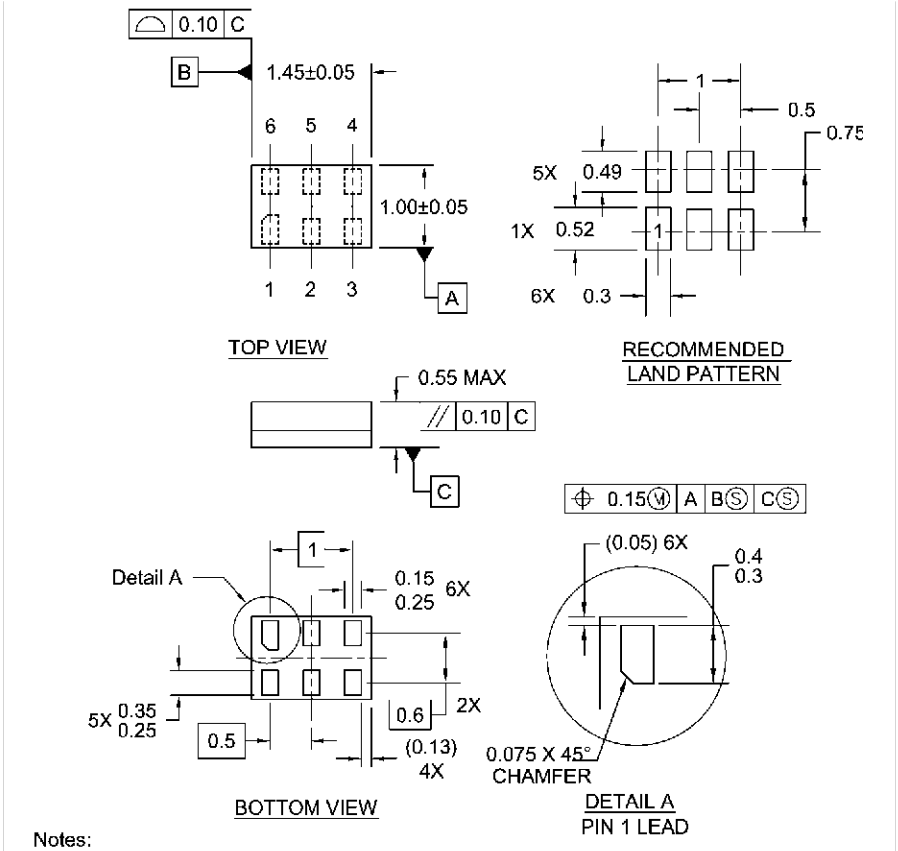
NOTES:

A. CONFORMS TO EIAJ REGISTERED OUTLINE DRAWING SC88A.
B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
C. DIMENSIONS ARE IN MILLIMETERS.

MAA05ARevC

5-Lead SC70, EIAJ SC-88a, 1.25mm Wide
Package Number MAA05A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Notes:

1. JEDEC PACKAGE REGISTRATION IS ANTICIPATED
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06ARevB

6-Lead MicroPak, 1.0mm Wide
Package Number MAC06A

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative